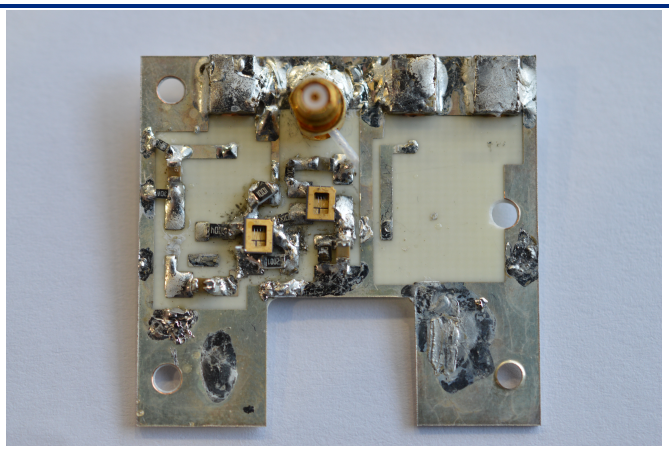
Cryogenic Low Noise Amplifier for Noise Spectroscopy in Scanning Tunnelling Microscopy



THESIS

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Author :	Corné Koks
Student ID :	2071541
Supervisor :	Dr. Milan P. Allan
2^{nd} corrector :	Prof. Dr. Jan M. van Ruitenbeek

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Cryogenic Low Noise Amplifier for Noise Spectroscopy in Scanning Tunnelling Microscopy

Corné Koks

Huygens-Kamerlingh Onnes Laboratorium, Universiteit Leiden
P.O. Box 9500, 2300 RA Leiden, The Netherlands

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Abstract

The low noise amplifier from Bastiaans et al. [1] is improved by increasing the bandwidth, such that measurement time is reduced. Instead of a single common-source transistor, a cascode setup is used. A common-source is followed by a common-gate which is followed by a common-drain. The gain (V/V) of the amplifier is estimated to be 22. The cascoding reduces the miller capacitance from 22pF to approximately 2pF. The input noise current is estimated to be 19fA/$\sqrt{\text{Hz}}$ and the voltage noise 0.2nV/$\sqrt{\text{Hz}}$. The power dissipation is estimated at 2mW.

Contents

Chapter 1

Introduction

1.1 Shot noise

Usual Scanning Tunneling Microscopy (STM) measurements are used for example to measure the pair breaking gap in supercondutors. This is done by measuring the current as a function of the bias voltage, where is latter is varied. The conductance as a function of bias voltage is related to the density of states. This technique is called Spectrospopic Imaging STM (SI-STM). High frequency fluctuations in the current are averaged out. However, these fluctuations contain information. For example, shot noise measurements contain information about the charge of the charge carriers. This technique is called Local-Noise Spectroscopy (LNS).

Using LNS, one can measure the charge of quasi-particles. If electrons tunnel randomly, the noise is called poissonian. In some exotic mesoscopic systems, the noise can be superpoissonian, which for instance Andreev reflections in superconductivity where two or more electrons are clustered [2]. Suppossionian noise means that charge carriers of less than one electron can tunnel [3][4]. With the first generation of cryogenic Low Noise Amplifier (cryo-LNA), charge trapping in the c-axis of BSSCO is measured [5]. Fano factors more than 30 are measured, which indicates that the c-axis is truly insulating, despite its zero resistivity below the critical temperature.

1.2 Cryogenic amplifier

In the past, cryogenic Low Noise Amplifiers (cryo-LNAs) have been proposed for STM measurements [6] or measuring Shot Noise [7] in meso-

scopic systems. The noise power is given by $S_{SN} = 2qI$. In typical STM measurements, shot noise is in the order of $1\text{fA}/\sqrt{\text{Hz}}$. Measuring this is a challenge, because the other noise sources need to be suppressed as much as possible.

To reduce the effect of the $1/f$ noise, a LC resonator has been proposed by DiCarlo et al. [8], on which the circuits of Bastiaans et al. [1] and Massee et al. [9] are based. The noise from the transistor is also of importance. Most commonly, commercial Avago Technology High Electron Mobility Transistors (HEMTs) are used because they are cheap and work at low temperatures [8][10][11][12]. Other transistors are also available which have much better noise characteristics [13].

Another point of interest for amplifiers is increasing the Gain Band-Width product (GBW). As described by Analui et al. [14], the largest GBW for transimpedance amplifiers is achieved by reducing the capacitance. This reduction of capacitance can be done using bootstrapping with positive feedback [15][16] or using cascoded design. Cascoding is an old and common technique, first proposed for in vacuum tubes by Hunt and Hickman [17] in 1939. It is often used in all types of circuits, for instance in cryo-LNAs [11][12][18]. This report focussus mainly on these two concepts.

A technique commonly used for on-chip transport measurements (quantum dots, break junctions) is impedance matching [19] [20], where the impedance of a junction is transformed to the 50Ω impedance of the coax cable. For STM, the junction impedance ($\gg 100\text{M}\ \Omega$) is much larger than for quantum dots ($<1\text{M}\Omega$) which makes it a challenge. An attempt for impedance matching in STM have been done by Kamiktarak et al. [21]. Impedance matching is most useful for reflectance measurements, such that junction impedance can be measured rapidly. However, for shot noise measurements, it is less useful. This is therefore not covered in this report.

1.3 Outline

In the theory section, the noise sources are described in more detail. Then, the key concept of this report, the LC resonator is described extensively. Finally some basics concepts in electronics are given, among which transistor setups and impedance matching.

The third chapter describes the ideas stated above in more detail, together with analytic derivations and simulations to show their expected performance. Cascoding and bootstrapping are covered in most detail, since those are the most extensively tested concepts. The use of a switch is described in less detail.

The fourth chapter is devoted to describe the details of the circuit which is used eventually, together with some drawings of the implementation of the circuit in the STM.

The fifth chapter describes the results of the tests on cascoding and bootstrapping. The sixth chapter would show the results of the cryogenic tests of the final amplifier. Unfortunatly, the amplifier is still under construction, so only estimations of the performance are given.

Chapter 2

Theory

This chapter first describes various noise sources. Then, the LC resonator is described. Then, some concepts in electronics are described, among which that transistor setups, impedance matching and the Barkhausen stability criterion.

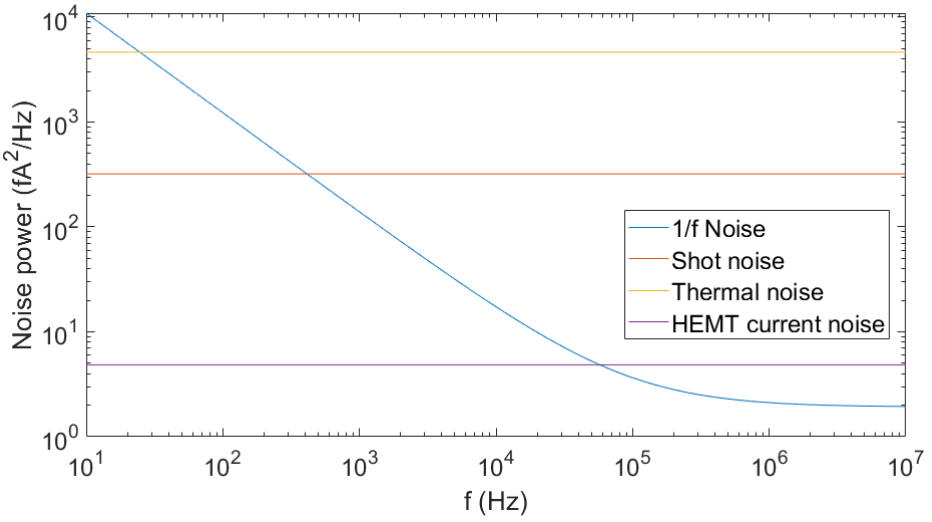

Figure 2.1: *The approximate current noise power is given below. The 1/f noise is a rough estimate, based on mechanical vibrations and voltage noise in the transistor. The cut-off of the 1/f noise is where the transistor voltage noise becomes predominantly white. The shot noise is based on a current of 100mA and poissonian noise. The thermal noise is based on a real impedance of 500kΩ. The HEMT current noise is 2.2fA/$\sqrt{Hz}$.*

2.1 Noise

The shot noise, thermal noise, 1/f noise and transistor noise sources are described.

Figure 2.1 gives an approximate noise power for each noise source. The 1/f noise is a rough estimate of the mechanical and transistor noise. The figure shows that from about 100kHz, the 1/f becomes small. This is thus the preferred region of doing the measurements. Note that the thermal noise is the dominant noise source in the setup.

2.1.1 Shot noise

The equation for shot noise is given by

$$S = 2|q|\langle I\rangle F, \tag{2.1}$$

where q indicates the effective charge and F indicates the Fano factor. For transport measurements, this Fano factor is given by

$$F = \frac{\sum_n T_n(1-T_n)}{\sum_n T_n}. \tag{2.2}$$

The full derivation is given in appendix A.1. Here, the Landauer approach is used, where single charge carriers have a finite probability for transmitting or reflecting through the barrier. For STM measurements, $T_n \to 0$ and thus $F \approx 1$.

An increase in shot noise, compared to normal metals can still be observed in STM. This because of an increase in effective charge. Cooper pairs have $|q| = 2e$ so that noise would double. Andreev reflections for STS junctions can give even high order of noise increment, i.e. $|q| = ne$ for some positive integer n.

2.1.2 Thermal noise

Thermal noise originates from the thermal equilibrium of two element, derived by Johnson and Nyquist [22]. Important is that only dissipative elements produce thermal noise, i.e.

$$S = 4k_bT\mathrm{Re}[Z]. \tag{2.3}$$

Imaginary parts do no contribute. This is important, because if the absolute value is considered, the sides bands of a LC-resonator would give an overestimation of the thermal noise.

Massee et al. [9], who have developed a circuit similar to Bastiaans et al. [1], report a thermal noise value of $S = 4k_bT|Z|_{max}$. For the LC resonator used in their circuit, this suggests a noise of $S = 4k_bT\frac{\omega_{res}^2L^2+R^2}{R}$. When the real value is considered, the thermal noise is given by $S = 4k_bT\frac{\omega_R}{\omega_{res}^2L^2+R^2}|Z(\omega)|^2$. The therm in the fraction does not change munch around the resonance frequency, but the impedance, $|Z(\omega)|$ does change significantly. Away from the resonance frequency it is thus important to consider the real part instead of the maximum impedance. More details are described in section 2.2 and appendix A.2.

2.1.3 1/f noise

Flicker noise is a general concept which is also applied to for instance earthquakes of the stock exchange. Key is that large events happen rarely and smalls event occur more frequently. For instance, in a semiconductor device there are many small traps, but a few large ones. The 1/f noise of the transistor is not of much relevance at 3MHz, since it is dominated by the white noise sources of the transistor, as shown in figure 2.1.

2.1.4 Transistor noise

The transistor noise is modelled as a voltage and current noise at the gate. Dong et al. [13] have fabricated a HEMT with much better noise characteristics than commercial HEMTs. One major noise factor is due to inelastic scattering, given by $S_{tr_v} = \frac{F2eI_{ds}}{g_m^2}$. From this one can see that reduction of impurities ($T_n \rightarrow 1$) reduce the noise of the transistor. This is dong by using Molecular Beam Epitaxy (MBE) growth.

Typical values for the transistor from Dong et al. [13] are a current noise of 2.2fA/$\sqrt{\text{Hz}}$ and a volage noise of 0.2nV/$\sqrt{\text{Hz}}$. These values are reported in appendix C. From Zavjalov [11] et al. the current noise for a commercial transistor (ATF33143) is 11.8fA/$\sqrt{\text{Hz}}$ and voltage noise of 1.3nV/$\sqrt{\text{Hz}}$.

2.2 LC resonator

The key concept of the amplifier is the LC resonator. Its characteristics are over covered in this section. The equivalent circuit is given by figure 2.2.

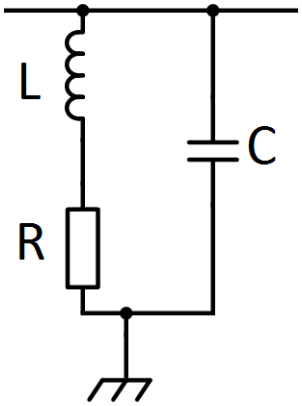

Figure 2.2: *Equivalent model of LC resonator.*

The impedance of this circuit is given by

$$Z_{LC} = (j\omega C - \frac{j\omega L}{\omega^2 L^2 + R^2} + \frac{R}{\omega^2 L^2 + R^2})^{-1}. \tag{2.4}$$

With inductance L, capacitance C and resistance R. For large enough Q-factors, $\omega^2 L^2 \gg R^2$, and equation 2.4 can be simplified. Furthermore, one can define the Q-factor as $Q = \frac{\omega L}{R}$. Using this, equation 2.4 becomes

$$Z_{LC} = (j\omega C - \frac{j}{\omega L} + \frac{1}{\omega L Q})^{-1}. \tag{2.5}$$

2.2.1 Impedance and bandwidth

The Q-factor is defined as

$$Q = \frac{f_0}{\Delta f}, \tag{2.6}$$

which thus contains a definition of bandwidth. The bandwidth Δf is the Full Width Half Maximum (FWHM) bandwidth. To get more insight into equation 2.4, it is best to normalised it to form

$$Y_{LC} = \sqrt{\frac{C}{L}}(\frac{j\omega}{\omega_0} - \frac{j\omega_0}{\omega} + \frac{\omega_0}{\omega Q}) = \sqrt{(\frac{C}{L})}(\frac{j\omega}{\omega_0} - \frac{j\omega_0}{\omega} + \frac{\Delta\omega}{\omega}). \tag{2.7}$$

For $\omega = \omega_0 + \frac{1}{2}\Delta\omega$, the admittance becomes $Y_{LC} = \sqrt{(\frac{C}{L})}(\frac{j\Delta\omega}{\omega_0} - \frac{\Delta\omega}{\omega})$. Here, the real and imaginary part are equal, which indeed corresponds to the $-3dB$ point.

Thus equation also shows that the maximum impedance is

$$Z_{LC} = \sqrt{\frac{L}{C}}Q = Q\omega_0 L. \tag{2.8}$$

However the FWHM ($\Delta\omega$) bandwidth is not useful for our purposes. More useful for a bandwidth is equating this to a certain impedance smaller than $Q\omega_0 L$. A certain impedance $\tilde{Z}$ now defines the bandwidth. This requires solving

$$(\frac{1}{\tilde{Z}}\sqrt{\frac{L}{C}})^2 = (\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega})^2 + (\frac{\Delta\omega}{\omega})^2. \tag{2.9}$$

The derivation is given in appendix A.3. The bandwidth is

$$BW = \sqrt{\frac{1}{(\tilde{Z}C)^2} - \Delta\omega^2} \tag{2.10}$$

around the frequency

$$\tilde{f}_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} + \frac{1}{(\tilde{Z}C)^2}}. \tag{2.11}$$

The minus sign in 2.10 in front of $\Delta\omega^2$ seems counter intuitive. However, a finite Q-factor reduces the impedance of the resonator and thus decreases the bandwidth.

For the amplifier, the SNR is of the form $SNR = \frac{S_i|Z_{LC}|^2}{S_i|Z_{LC}|^2+S_v}$, where S_i is the current noise and S_v is the voltage noise. If the impedance, $\tilde{Z}^2 = \frac{S_v}{S_i}$, is defined as the ratio of noises and the maximum impedance, $Q\omega_0 L$ is much larger than $\tilde{Z}$, then the bandwidth, BW, defines the FWHM of the SNR. This is the main figure of merit which needs to be maximised.

2.2.2 Mechanical analog

To get a more intuitive idea, it is useful to convert the electrical circuit to a mechanical analogue. The LC resonator can easily be mapped to a pendulum. By writing the Kirchhof Current Law (KCL), one arrives at

$$(jwC + \frac{1}{jwL} + \frac{R}{w^2L^2})v = i_{ext} \tag{2.12}$$

or equivalently, with $v \equiv \dot{q}$ in the time domain,

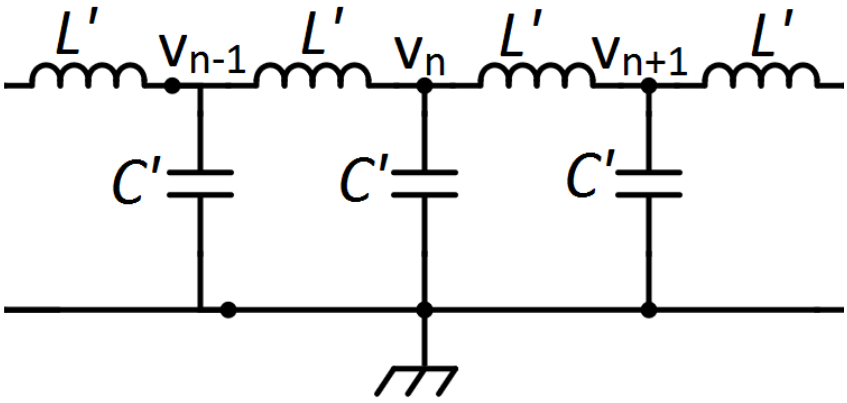

Figure 2.3: *Model of some part of transmission line. L' and C' denote the inductance and capacitance per length. v_n is the voltages at some each node.*

$$C\ddot{q} + \frac{q}{L} + \int \frac{R}{L^2} q \mathrm{dt} = \ddot{q}_{ext}. \tag{2.13}$$

The last equation already looks like a harmonic oscillator with strange damping therm. With the equation of motion for a mass spring system

$$m\ddot{x} + kx + \gamma\dot{x} = F_{ext}, \tag{2.14}$$

the capacitance can be mapped to the mass, the inductance to $\frac{1}{k}$.

Another interesting point is that the KCL for a transmission line like structure, shown by figure 2.3, is in the mechanical analogue given by

$$C'\ddot{q}_i + \frac{1}{L'}(2q_i - q_{i-1} - q_{i+1}) = 0, \tag{2.15}$$

where L' and C' are the inductance and capacitance per unit length. Equation 2.15 is equivalent to the of phonons for a 1D piece of material. The characteristic impedance for acoustic waves is given by $z = \rho v_s$. The density $\rho = \frac{Am_i}{Ab}$, where b is a lattice vector, m_i is the mass of a single atom and A is the perpendicular surface. The velocity of sound is $v_s = b\sqrt{\frac{k}{m}}$. The acoustic impedance is thus $z = \sqrt{km}$ and the electrical analogue is $Y = \sqrt{\frac{C'}{L'}}$. This is not the electrical impedance, but the admittance. As described later in 2.4, the reflectance is given by $\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$. In therms of admittance, it is equal apart from a sign change: $\Gamma = -\frac{Y_L - Y_0}{Y_L + Y_0}$ *. A typical coaxial cable has $\sqrt{\frac{L'}{C'}} = Z_0 = 50\Omega$ as a characteristic impedance.

*The point is that it is ambiguous to call something an admittance of impedance.

2.3 Transistor setups

A transistor can be considered as a three port device; gate, drain and source. In practise, two ports act as in- and output for the signal, while the third is grounded for AC signal. The part which is AC grounded is called common X (it is not necessarily grounded, but in practise this is most commonly done). In the following subsections, their simplistic models are given, together with key equations. Important to keep in mind is that the gate is not completely disconnected from the drain and source. There is a gate-source and gate-drain capacitance of typically a few picofarad, which influences the input impedance. † In the following figures and equations, v_g,v_s and v_d indicate the gate, source and drain voltage (AC). C_{GD} and C_{GS} are the gate-drain and gate-source capacitance respectively. g_m is the transconductance, which determines alternating current in the modelled current source as $i = g_m(v_g - v_s)$.

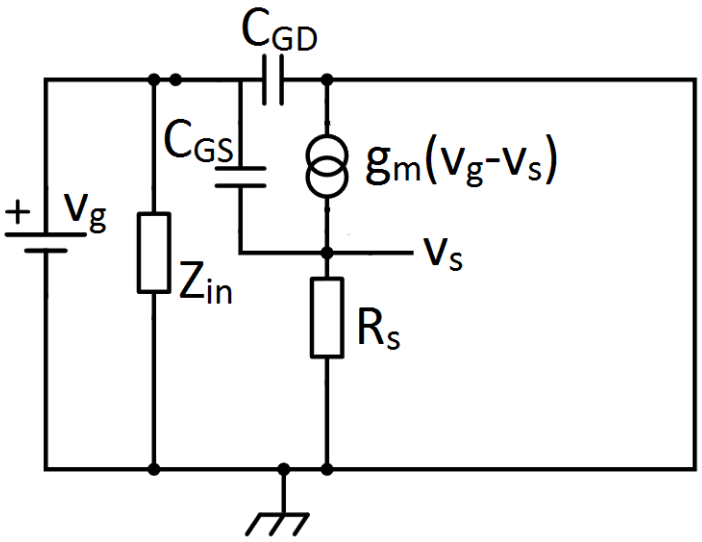

Figure 2.4: *Equivalent circuit of CD transistor. V_g is the input voltage, V_s is the output voltage.*

When mapping to a different system, switching from admittance to impedance of v.v. does not matter for waveguides.

†From the key equation for MOSFET transistors: $I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{thr})^2$ and $g_m \equiv \frac{dI_{DS}}{dV_{GS}}$ one can see that transconductance and parasitic capacitance are proportional.

2.3.1 Common drain

The common drain (CD or source follower) amplifies signals from the gate towards the source. Its equivivalent circuit is given in figure 2.4. This amplification is given by

$$A = \frac{v_s}{v_g} = \frac{R_s}{r_m + R_s}, \tag{2.16}$$

where $r_m = \frac{1}{g_m}$. The AC current through the transistor is determined by the difference between gate and source voltage. The source voltage is thus $v_s = R_s g_m (v_g - v_s)$ which solves to equation 2.16. The input impedance is given by

$$Z = Z_{in} || \frac{1}{j\omega C_{gd} + j\omega C_{gs}(1 - \frac{R_s}{r_m + R_s})}. \tag{2.17}$$

Where $||$ indicates a parallel configuration, i.e. $a||b = \frac{ab}{a+b}$. Note that the gate-source capacitance is effectively reduced, because the voltage at the gate and the source are proportional and in phase with each other. The drain is grounded, so there is no change there.

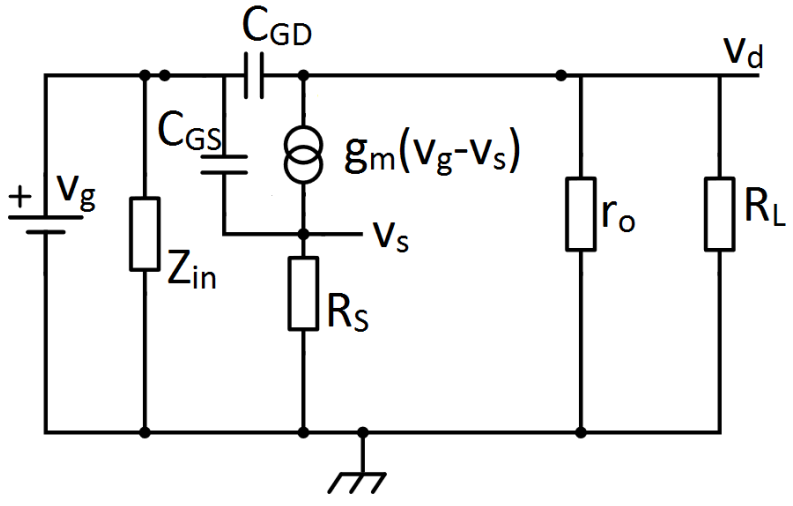

Figure 2.5: *Equivalent circuit of CS transistor. V_g is the input voltage, V_D is the output voltage. Technically, r_o should be connected between v_d and v_s, but for large gains, this figure is approximately correct.*

2.3.2 Common source

The common source (CS) transistor is similar to the CD, except the drain is the output. The output is thus at the other side of the current source resulting into a opposite phase. Solving the equations $v_s = R_s g_m(v_g - v_s)$ and $v_d = (r_o||R_L)g_m(v_g - v_s)$ gives the gain equation

$$A = \frac{v_d}{v_g} = -\frac{r_o||r_D}{r_m + R_s}. \tag{2.18}$$

Commonly, the source is grounded which gives a gain of $A = -g_m(r_o||R_L)$. The input impedance is now given by

$$Z = Z_{in}||\frac{1}{j\omega C_{gd}(1 + \frac{r_o||r_D}{r_m+R_s}) + j\omega C_{gs}(1 - \frac{R_s}{r_m+R_s})}. \tag{2.19}$$

The gate-source capacitance is corrected for, like in the CG. The gate-drain capacitance now also has a correction factor, but with an opposite sign. Due to the π-phase difference, the capacitance is effectively enlarged. This is known as the miller effect. This effect can be reduced, as will be described in section 2.3.4.

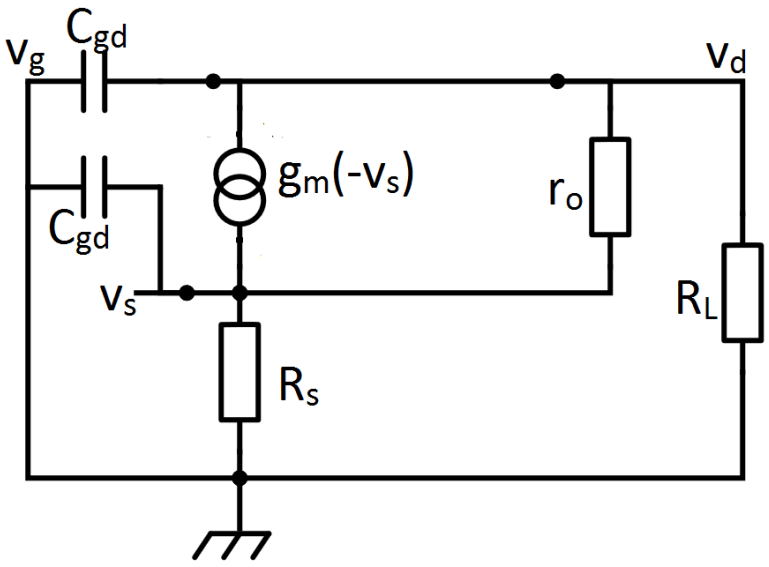

Figure 2.6: *Equivalent circuit of CG transistor. v_s is the input voltage, v_d is the output voltage. v_g is grounded.*

2.3.3 Common gate

The third type is the common gate. Here the source is the input and the drain is the output. Figure 2.6 shows that the total current through the transistor is given by $i_{DS} = g_m v_s - \frac{v_d - v_s}{r_o} = \frac{v_d}{R_L}$ so that the gain is given by

$$A = \frac{v_d}{v_s} = (g_m + \frac{1}{r_o})R_L||r_o \approx g_m(R_L||r_o). \tag{2.20}$$

The input impedance can be determined using $v_s = r_o(i_{DS} - g_m v_s) + i_{DS}R_L$ which is the voltage drop over the load and the internal resistance of the transistor. Together with the capacitors, the input impedance is

$$Z = R_s||\frac{1}{j\omega C_{GS}}||(\frac{R_L||\frac{1}{j\omega C_{GD}} + r_o}{1 + g_m r_o}). \tag{2.21}$$

The input impedance is approximately $Z = r_m \frac{R_L + r_0}{r_0}$.

2.3.4 Cascoding

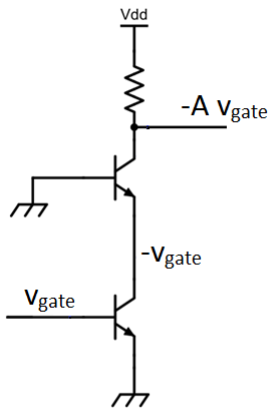

Figure 2.7: *The gate voltage is amplified by the first HEMT in the CS setup, which is then amplified by the CG stage. The first stage is assumed to have a small, in this can unity gain. The second stage provides the desired large gain.*

Cascoding is an old concept invented in 1939 by Frederick Vinton Hunt and Roger Wayne Hickman [17]. A cascode amplifier has a CD or CS with

a CG stacked on it. The CS with CG cascode setup is used to have a reduced miller effect.

From equation 2.19, the capacitance is effectively enlarged by the gain. The input capacitance is approximately given by

$$C_{tot} = C_{GS} + (A+1)C_{GD}. \tag{2.22}$$

For large gains, the input capacitance is substantially increased. For a gain of 30 and a gate-drain capacitance of 1pF, the additional capacitance, or miller capacitance, is 30pF. This effect can be reduced by the setup as schematically shown in figure 2.7.

This first stage has a gain of unity. The miller capacitance is thus only 1pF. The common-gate transistor then amplifies the signal. The amplification is thus 'delayed' to the second stage.

One needs to take into account an additional noise source in the CG transistor. The gate is grounded, but still contain some noise. This can also be modelled to be a noise source at the source, because only the voltage difference between the source and the gate is of importance. If the gain of the first stage (the CS) is too small, the signal between the two transistors will be dominated by the aforementioned noise. Therefore, a gain of about unity should be chosen.

2.4 Impedance matching

Impedance matching is important when the signals are considered to be waves. The wavelength (in vacuum) is given by $\lambda = \frac{c}{f}$, where c, so for 3 MHz, the wavelength is 100m. Typically, for structures $l < \frac{\lambda}{20}$, the wave-like behaviour is important.

Key is to maximise the power over the load. If one considers a simple circuit from figure 2.8, the power is given by

$$P = I^2 Z_L = V^2 \frac{Z_L}{|Z_L + Z_0|^2}. \tag{2.23}$$

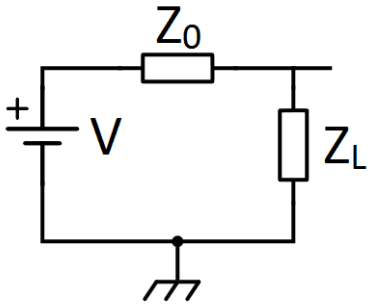

Figure 2.8: *Equivalent circuit of impedance matching. Z_0 indicates the impedance of a transmission line. Z_L is a load impedance.*

Maximising this with respect to Z_L gives the condition $Z_L = Z_0^*$. The impedance of the cable Z_0 is a constant, most commonly 50Ω.

To appreciate impedance matching better, lets first consider a one port device. In contrast to basic electronics, one has to consider forward and backward moving waves, given by v^+ and v^- respectively. This gives equations

$$\begin{aligned} v^+ + v^- &= iZ_L \\ v^+ - v^- &= iZ_0 \end{aligned} \tag{2.24}$$

which gives the reflection coefficient

$$\Gamma \equiv \frac{v^+}{v^-} = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{2.25}$$

Equations 2.24 look strange, but can be understood by considering Z_L to be infinitesimally small and Z_0 to be infinitely long. For ideal lumped elements (zero length), the wavelike behaviour does not matter. Therefore, the voltage can be consider to be "point-like", i.e. $v = v^+ + v^-$. The coax cable is designed as a wave guide so the wavelike behaviour is crucial This means that the direction of voltage is proportional to the transmitted current, i.e. $\tilde{v} = v^+ - v^-$.

2.4.1 Finite length transmission line

If the transmission line length is comparable to the wavelength of the voltage waves, so the equations become more complicated. From an ideal transmission line (no losses), its equations are given by

$$\begin{aligned} dv(z,t) &= -dz\omega L' di \\ di(z,t) &= -dz\omega C' dv \end{aligned} \tag{2.26}$$

resulting in the wave equations

$$\begin{aligned} v(z) &= v^+ \exp^{-j\omega\sqrt{L'C'}z} + v^- \exp^{j\omega\sqrt{L'C'}z} \\ i(z) &= i^+ \exp^{-j\omega\sqrt{L'C'}z} + i^- \exp^{j\omega\sqrt{L'C'}z} \\ &= \frac{v^+}{Z_0} \exp^{-j\omega\sqrt{L'C'}z} - \frac{v^-}{Z_0} \exp^{j\omega\sqrt{L'C'}z}. \end{aligned} \tag{2.27}$$

The input impedance is given by

$$Z_{in}(z) = \frac{v(z)}{i(z)} \tag{2.28}$$

The forward and backward travelling waves are determined by the way the transmission line is terminated. The relation between v^+ and v^- is given by equation 2.25. The input then becomes

$$Z_{in} = Z_0 \frac{Z_L - jZ_0 \tan(\omega\sqrt{L'C'}d)}{Z_0 - jZ_L \tan(\omega\sqrt{L'C'}d)}. \tag{2.29}$$

Where d is the length of the transmission line, $Z_0 = \sqrt{\frac{L'}{C'}}$ and Z_L are again the characteristic impedance of the cable and the load which terminates the cable. Obviously, if the transmission line is terminated with 50Ω, the input impedance is also 50Ω. Also note that for $\omega\sqrt{L'C'}d \ll 1$, the length is irrelevant and the impedance is just $Z_{in} = Z_L$.

The unpredictable wavelike behaviour thus does not appear if the cable is much shorted than the wavelength, or if the cable is therminated by 50Ω.

2.5 Barkhausen stability criterion

The Barkhausen stability criterion is an obvious restriction on a feedforward system. It is explained for the Wien bridge in Martinez-Garcia et al. [23] which explains where the Wien bridge forms an oscillator and when it is unstable. The theory holds more generally.

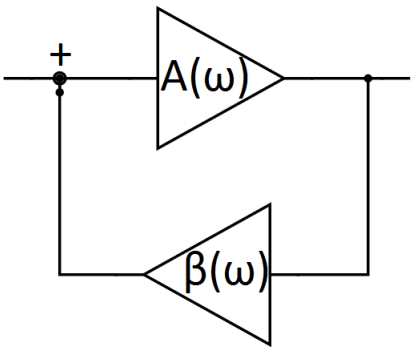

Figure 2.9: *Stability figure of feedforward systems. The input signal arriving from the left gets amplified and voltage divided, such that a signal multiplied with $A\beta$ is added to the input.*

Consider a feedforward system as given by figure 2.9, the voltage v_0 is amplified by a factor A and voltage divided with a factor β (note that both A and β can be functions of frequency. The Barkhausen criterion states that stable oscillations occur if the following two conditions are satisfied

$$\begin{aligned} |A\beta| &= 1 \\ \measuredangle(A\beta) &= 0. \end{aligned} \tag{2.30}$$

If practise $|A\beta| > 1$ for some frequency and hence the unstable solution.

Chapter 3

Simulations

In this chapter, first the circuit from Bastiaans et al. [1] is explained. Then, the main conditions for the simulations are explained, in which the last mentioned circuit is the standard which is improved. The improvement using cascoding and bootstrapping is explained. Last, the advantages and disadvantages of using a switch are discussed.

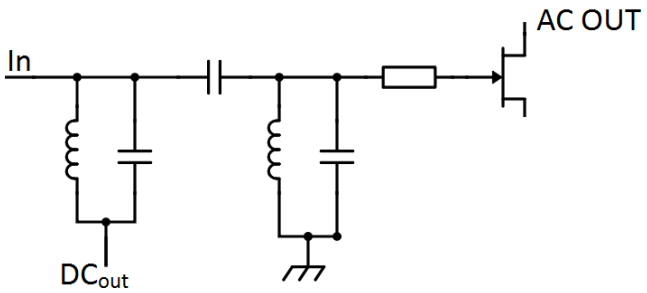

Figure 3.1: *The basic idea of the amplifier. Two tank circuit are separated by a capacitor. The left tank and the capacitor act as a Bias Tee. The capacitance in the tank is a parasitic of the inductor, so not a mounted element. IN is the total input signal, i.e. the tunneling current. The DC OUT line goes to the feedback electronics of the STM. AC OUT is the signal for the noise measurements.*

3.1 Amplifier as proposed by Bastiaans et al. [1]

The amplifier described in Bastiaans et al. is mostly based on DiCarlo et al. [8]. The high frequencies (2MHz) are measured using an LRC resonator, where the capacitance is mostly due to the coax cable. The proposed amplifier by Bastiaans et al. does not have this parralel resistor, such that the

impedance is larger. Part of the circuit is given by figure 3.1.

Two frequencies ranges are of importance. The main focus of this report is the high frequency range which is about 5MHz. At this high frequency range, the capacitor between the tanks is approximately a short. This gives an effective inductance of $L_{eff} = L/2$ and a capacitance of $C_{eff} = 2C$. The values for the tank inductance L and the tank capacitance C are 66μH and 15pF, respectively. The resonance frequency is therefore given by $f_{res} = \frac{1}{2\pi}\frac{1}{\sqrt{LC}}$, which is approximately 5MHz. The amplifier proposed by Bastiaans et al. also report a cable capacitance of 30pF. In the new amplifier this value is expected to be much smaller, to about 4pF. For simplicity, this is included in the tank capacitance.

The other frequency range is about 1kHz. This is the range where $\frac{\mathrm{d}I}{\mathrm{dV}}$ measurements are performed. Current going through the left tank and thus to DC OUT goes to the feedback electronics of the STM. It is important that the current goes through the first tank such that STM feedback electronics receive the most signal. The ratio between the two currents is equal to the ratio of impedances, given by

$$\frac{Z_1}{Z_2 + Z_c} = \frac{-\omega^2 L C_c}{1 - \omega^2 L(C + C_c)} \approx -\frac{\omega^2}{\omega^{*2}}. \tag{3.1}$$

where $\omega^* = \frac{1}{\sqrt{LC_c}}$. So if C_c is too large, the ratio goes to one and only half the current will flow through the first tank. If the ratio is too large, the signal is well separated, but high frequency signals can't pass through the second tank.

Note that this ratio also holds for signals at the input of the transistor, i.e. at the input of the right tank. So the input current noise of the transistor will not pass through the left tank and no additional noise source is added to DC OUT.

3.2 Rules for simulations

In all simulations given below, the following conditions are taken into account. First of all, the temperature is 4.2K, the DC current which gives rise to shot noise is 100pA and charge carriers are taken to be single electrons, i.e. $|q| = e$. The schematic of the simulations is given by figure 3.2. In both tanks; the inductance is 66μH, the capacitance is 15pF, the Q-factor is 600 and the resistance is thus $R = \left.\frac{2\pi f L}{Q}\right|_{f=3MHz} \approx 2.1\Omega$. The transistor is assumed to have noise values of $2.2\mathrm{fA}/\sqrt{\mathrm{Hz}}$ and $0.2\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (appendix C).

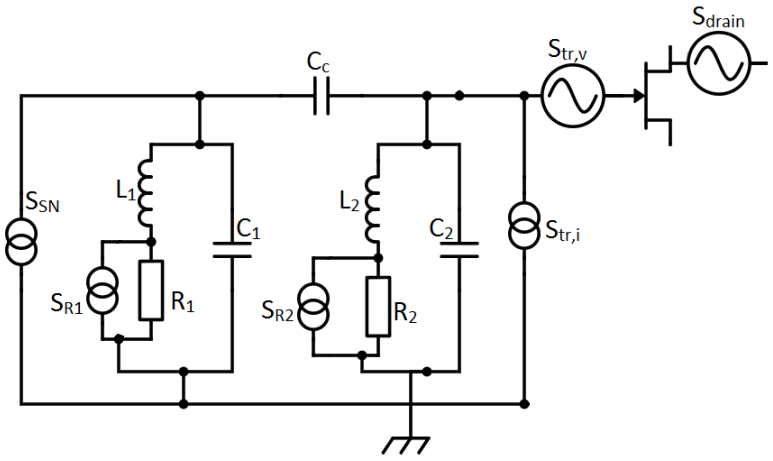

Figure 3.2: *The equivalent circuit for the noise simulations is given here. The noise at the end of the drain of the transistor is due to the thermal noise of the drain resistor.*

The capacitance of the coaxial cable from STM to circuit is assumed to be negligible, i.e. the total input capacitance if 15pF which is the capacitance of the first tank.

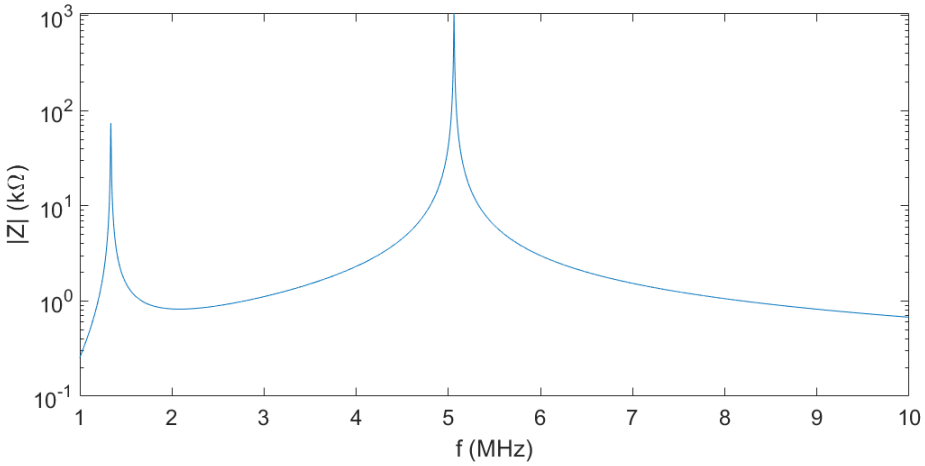

Figure 3.3: *Two peaks are visible. The low frequency peak corresponds to the even mode, the high frequency peak to the odd mode. The high frequency peak is used.*

Figure 3.3 shows the impedance of both tanks. That is, any current first arriving at the left tank, results in a voltage at the gate such that the vertical axis in figure 3.3 is defined as $|Z| = |\frac{v_{gate}}{i_{left}}|$. Two peak are visible

due to the coupling capacitor. In practise, only the high frequency peak is used, because it has the largest impedance.

The total noise power arriving at the gate is shown in figure 3.4.

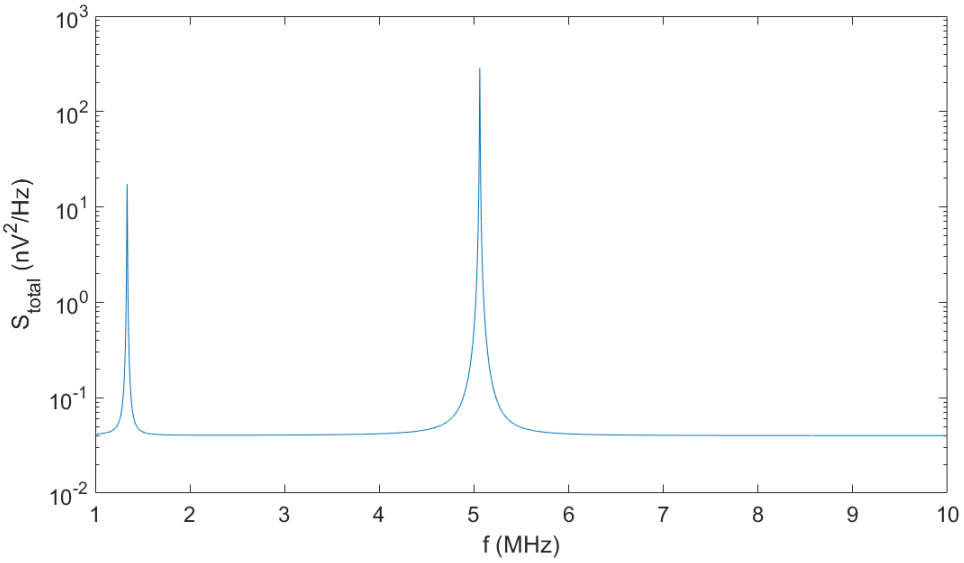

Figure 3.4: *The total voltage noise which arrives at the gate of the transistor. The noise floor is due to the transistor noise, $0.2nV/\sqrt{Hz}$.*

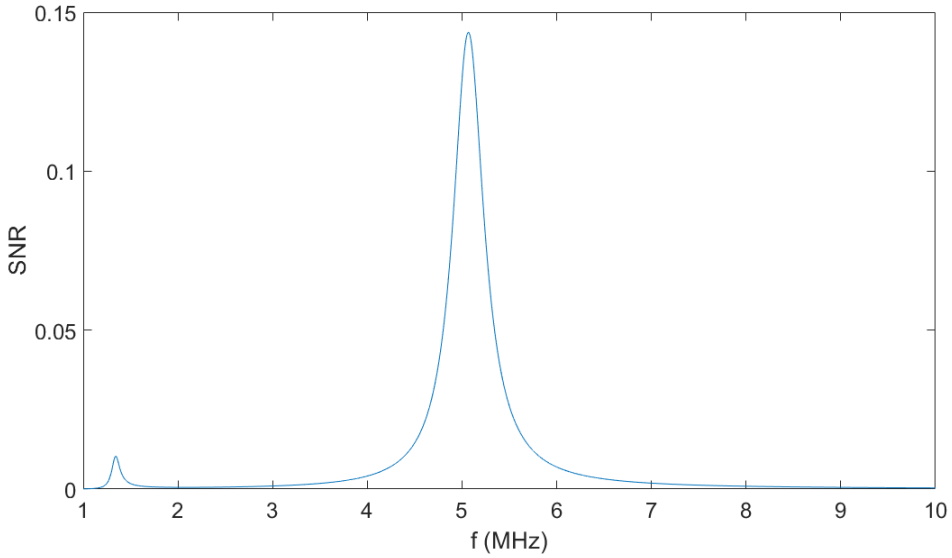

Figure 3.5: *The SNR as a function of frequency as defined in equation 3.2.*

More useful is the signal to noise ratio. This is defined as

$$SNR(f) = \frac{|ZI|^2 S_{SN,i}}{|ZI|^2 S_{tank1,i} + |ZII|^2 (S_{tank,i} + S_{tr,i}) + S_{tr,v}}, \tag{3.2}$$

where ZI is the impedance for any current arriving at the left tank and ZII is the impedance for any current arriving at the right tank, such that $ZI = \frac{v_{gate}}{i_{left}}$ and $ZII = \frac{v_{gate}}{i_{right}}$. At the gate of the transsitor, the SNR for each frequency is given by figure 3.5.

As was suggested in section 2.2.1, the bandwidth of the SNR is larger than the bandwidth of the impedance. In figure 3.6 both the impedance $|ZI|$ and the SNR are normalised to their maximum.

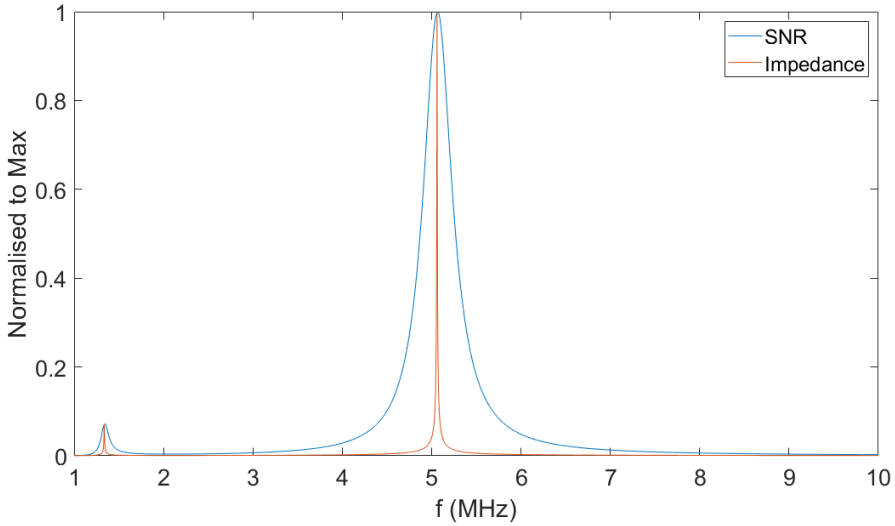

Figure 3.6: *Both SNR and impedance for currents arriving at left tank are normalised to one. One can see that the bandwidth is in fact larger for the SNR than for the impedance.*

3.3 Cascoding

3.3.1 Improved SNR and bandwidth

Cascoding mostly affect the circuit after the transistor. The main idea is that using a larger gain, a larger bandwidth can be measured without losing good SNR. The SNR was already given in equation 3.2, however, effectively, the SNR is given by equation 3.3. Here, one can see that for a small

gain, the SNR goes down. This is because the noise at the drain has less influence on the signal.

$$SNR(f) = \frac{A^2|ZI|^2 S_{SN,i}}{A^2|ZI|^2 S_{tank1,i} + A^2|ZII|^2(S_{tank,i} + S_{tr,i}) + A^2 S_{tr,v} + S_{drain}}. \tag{3.3}$$

If the drain part of the transistor is 50Ω, the voltage noise is $0.1\text{nV}/\sqrt{Hz}$. Even further, if gain is small, e.g. $A = 0.1$, the noise is effectively $1\text{nV}/\sqrt{\text{Hz}}$. Therefore, a large gain gives a better SNR.

A larger drain resistance implies a larger noise. However, this noise scale with $S_{noise} \sim R_D$ while the signal scales with $S_{signal} \sim A^2 \sim R_D^2$. The SNR for different drain resistors is given by figure 3.7.

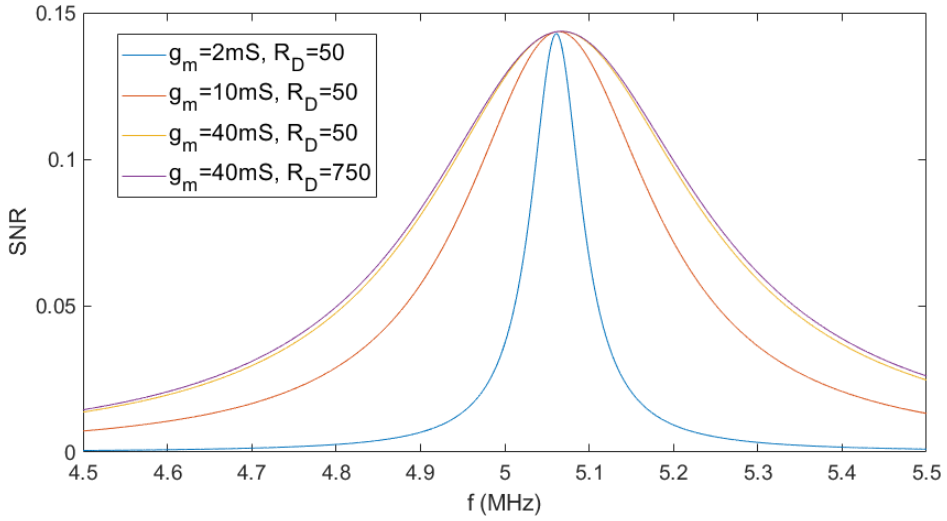

Figure 3.7: *The SNR for different transistor transconductances and drain resistors is shown. The gain is given by* $A = g_m R_D$.

The curve for $g_m = 2mS$ and $R_D = 50\Omega$ is a rough approximation of the old situation. One can see that the bandwidth is relatively small. Increasing the transconductance increases the bandwidth. The bandwidth is limited by the $0.2\text{nV}/\sqrt{\text{Hz}}$ voltage noise of the transistor. Figure 3.7 shows that for $g_m = 40mS$, a drain resistance of 50Ω and 750Ω shows no difference. The reason for using this larger than then necesary, is to eliminate other noise sources in the further amplification stages. These are

given by S_{extra}. *, the SNR is

$$SNR(f) = \frac{|ZI|^2 S_{SN,i}}{|ZI|^2 S_{tank1,i} + |ZII|^2 (S_{tank,i} + S_{tr,i}) + S_{tr,v} + \frac{S_{drain} + S_{extra}}{A^2}}. \quad (3.4)$$

This shows that also these extra noise sources effectively go down by a factor A^2.

Another noise source, which increases with frequency is the gate-drain capacitor. If this is about 1pF, the current noise is increased by $S_{drain,v}\omega^2 C^2$. In the cascode configuration, the input is more decoupled from the output, i.e. this noise source is expect to become less relevant. The voltage noise at the gate of the CG transistor is also added, which would include a noise of about $0.1\text{nV}/\sqrt{\text{Hz}}$. For simplicity in the simulations, this is included in the transistor noise, such that the total transistor noise is still $0.2\text{nV}/\sqrt{\text{Hz}}$.

3.4 Bootstrapping

Bootstrapping is the charging of discharging of any parasitic capacitance using an amplifier. When a capacitor is charged, the additional amplifier discharges the capacitor and v.v.. Effectively the capacitance is thus reduced, which increases the bandwidth of the SNR, as shown in equation 2.10.

The key element for bootstrapping is a non-inverting amplifier with a gain A larger than one. Birk et al. [15] use an external amplifier. For practical reasons, the amplifier is a PCB which also contains the feedback line, so there is no external amplifier. This has the advantage that the delay of the signal is smaller and thus the frequency of operation is larger. Birk et al. claim this is their major limitation in frequency range. As an example, if one would measure at frequencies of 30MHz, the wavelength is 10 meters. Therefore, to get a good signal, the amplification line needs to be much smaller than 10 meters. For a circuit on a chip, this should not give any problems. Figure 3.8 shows this setup, where the two CS transistor together form a non-inverting amplifier with gain A.

*This thus effectively lowers the noise floor of the Lock-In amplifier, which is used to measure the signal.

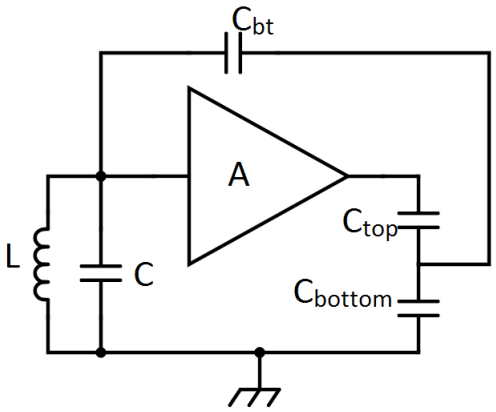

Figure 3.8: *A non-inverting amplifier, together with voltage divider* (C_{top}, C_{bottom}) *effectively reduce the capacitance C in the tank.*

Using the KCL for the input, like in section 2.2.2, the idea becomes more intuitive. In fact, the principle is the opposite of the miller effect, where the input capacitance increases. The KCL is given by

$$(j\omega C + \frac{1}{j\omega L} + \frac{R}{\omega^2 L^2})v = \sqrt{S_{SN,i}} + \sqrt{S_{th,i}} + j\omega C_{bt}((A-1)v + \sqrt{S_{drain,v}}), \tag{3.5}$$

or more suggestively

$$(j\omega(C-(A-1)C_{bt}) + \frac{1}{j\omega L} + \frac{R}{\omega^2 L^2})v = \sqrt{S_{SN,i}} + \sqrt{S_{th,i}} + j\omega C_{bt}\sqrt{S_{drain,v}}. \tag{3.6}$$

One can see that the capacitance is effectively reduced for a gain $A > 1$, to

$$C_{eff} = C - C_{bt}(A-1). \tag{3.7}$$

The complete noise equivalent circuit is given by figure 3.9. Where the noise of the drain comes from the drains of both amplification stages, where the first amplification stage causes the largest gain. [†] The noise at the drain is thus $S_{drain} = 8k_bTR_{D1}$. There is an extra noise therm given by $(\omega C_{bt})^2 S_{drain}$. The extra noise therm scales linearly in gain ($S \sim R_D \sim A$), but quadratically in C_{bt}. The effectively reduced capacitance scales

[†]The reason for choosing the first amplification stage to have the largest gate is the the total noise is given by $S = 4k_bTR_{D1}(g_mR_{D2})^2 + 4k_bTR_{D2}$. Together with $A = gmR_{D1}gmR_{D2}$, the noise is $S = 8k_bTAR_{D2}$. Minimising for R_2 thus gives the lowest noise. However, the second amplification stage is chosen to have unity gain and thus the thermal noise therm at the drain is given by $S = 8k_bTR_{D1} \equiv 8k_bTR_{drain}$

linearly in both capacitance and gain, so it is preferable to minimise the capacitance. Capacitors below 1pF are rare and therefore 1pF is chosen as the bootstrapping capacitance.

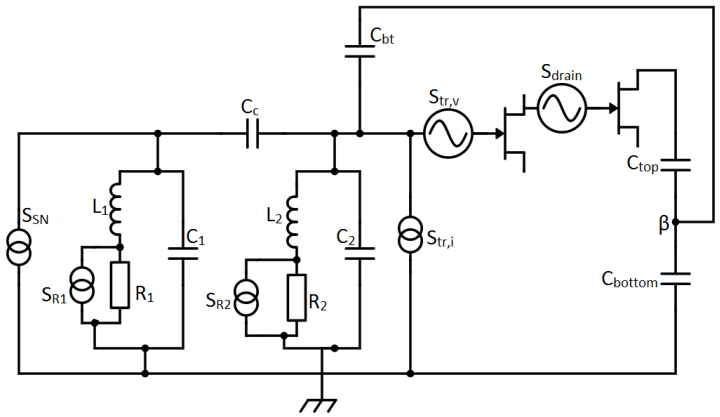

Figure 3.9: *Noise equivalent circuit for bootstrapping. Here, β is a voltage devider, which is for now assumed to be perfect. This means that only for the voltage dividing, C_{bt} is assumed to have an infinite impedance.*

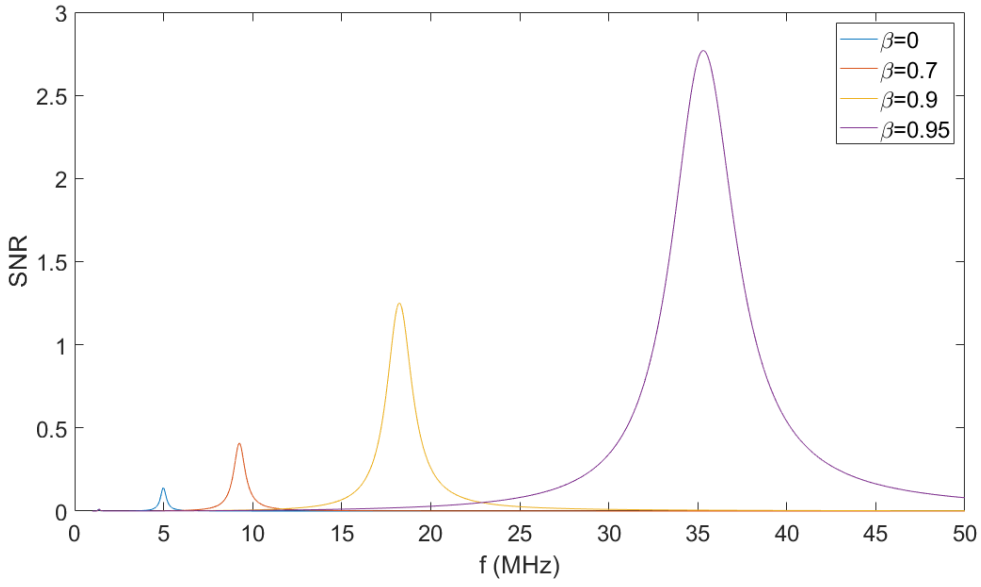

Figure 3.10: *For larger effective gains (larger β) the resonance frequency shift and also the impedance increases. This gives an improved SNR. The gain is 30, such that the effective capacitance is approximately $C_{eff} = 30pF - 30 \cdot \beta \cdot 1pF + 1pF$.*

In order to get some fine tuning in the system, the output voltage divided, using a variable resistance or a varactor. In order to not add any noise, the voltage divider is constructed with two capacitors C_{top} and C_{bottom} given rise to a voltage division ratio $\beta = \frac{C_{top}}{C_{top}+C_{bottom}}$. One of these capacitors should thus be a varactor diode, such that some control is achieved. The total gain is thus $A\beta$. Thus SNR for different voltage division ratios is given in figure 3.10.

This figure shows the major improvement in SNR. This is because the impedance is given by $Z_{LC} = \sqrt{\frac{L}{C}}Q$, so for small capacitors the impedance increases much. At some gain, the capacitance becomes negative (see equation 3.7) and the LC resonator stops working, which is at $A\beta = 1 + \frac{C}{C_{bt}}$. Figure 3.10 seems to suggest the critical value for β is 1. This is not the case, A is 30 in this case, so also for $\beta = 1$ the effective capacitance is still positive.

3.4.1 Limitations on bootstrapping

It is of importance for the bootstrapping to have a flat gain. That is, for every frequency, the drain resistance has to be constant. This is a challenge, since there is a capacitor in series with an LC-resonator, which gives rise to a zero. This is expressed by

$$Z_{drain} = R_D||(\frac{1}{j\omega C_{top}}\frac{1+\frac{C_{bt}+C_{top}}{C_{bottom}} - \omega^2 L(C + C_{bt} + \frac{CC_{bt}}{C_{bottom}} + \frac{C_{top}}{C_{bottom}}(C + C_b t))}{1 + \frac{C_{bt}}{C_{bottom}} - \omega^2 L(C + C_{bt} + \frac{CC_{bt}}{C_{bottom}})}). \tag{3.8}$$

The drain thus has a zero at

$$\omega_0^2 = \frac{1}{LC}(1 + \frac{C_{bt}}{C}\frac{C_{bottom} + C_{top}}{C_{bottom} + C_{top} + C_{bt}})^{-1} \approx \frac{1}{L(C + C_{bt})}. \tag{3.9}$$

Where the last approximation is for the voltage dividing capacitances to be larger then the tank capacitance. The appearance of the zero indicates that there is a frequency for which is the gain of the amplifier is zero. Note that the above two equations are approximations. The voltage at the gate is assumed to be independent of the input. For large gains, this approximation is valid. If C_{bottom} and C_{top} are large, this peculiarity should only appear at the lowest frequency and where gain is small and this equation is not valid i.e. the current would not flow over the resonator but over the

resistor [‡]. For larger gains, where it is valid, the frequency is well above this zero.

Another reason for a non-flat gain is low-pass filtering in the circuit. Typically, a flat gain can be created up too 100MHz (drain resistance of 500Ω and 3pF parralel capacitance). From frequencies higher than this, the bootstrapping would not work.

Birk et al. [15] claim the bootstrapping in their circuit breaks down because the amplification line is too large w.r.t. the wavelength of the signal. For a circuit on a PCB, the amplification line is about 5cm. Therefore, the circuit only breaks down for frequencies above 100MHz (ratio length and wavelength is there $\frac{0.05}{3}$ which should be sufficient for functioning bootstrapping).

3.5 Switch

In order to protect the transistor from static discharges or other effects, it could be usefull to implement a switch which disconnects the transistor circuit from the STM electronics.

A relais switch has been used by Robinson et al.[12], who created a very similar circuit for cryogenic environments. They reported a switching time of 1ms with a dissipation of less than 1 mJ. In their paper it was used to switch between an oscillator and external source.

In our case, the switch could be used to remove one inductor. Two inductors are necessary to make sure the noise from the transistor does not drop over the transimpedance amplifier. However, if we could fully separate the high frequency measurements and the regular measurements, the impedance could be doubled by using only one coil. The scheme is by figure 3.11.

For the regular measurements, the transistor has to be disconnected from the STM circuit, using 'S2'. A floating gate might harm the transistor, so the transistor has to be shorted to ground, using 'S1'. This is the configuration of figure 3.11.

[‡]The voltage at the input and output are approximately equal, so little current will flow over this.

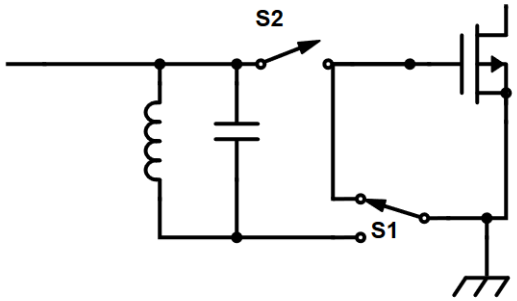

Figure 3.11: *The schematic of a switch diagram is given. This current setup would be for low-frequency measurements. If both switches are in the other direction, the high frequency measurement setup is shown.*

For the high frequency measurements, the coil has to be grounded to the same ground as the transistor, so 'S1' is flipped. 'S2' also has to be connected to the gate of course.

The downside of a switch is the additional capacitance towards the internal electronics of the relais. This capacitance will be in the order of pF which could give additional current noise (see section 3.4). Furthermore, each time a switch is switched, this capacitance can be slightly different, yielding a change in this noises and resonance frequency. Last, it was reported by [12] that the switching voltage has to be increased when used more often.

Chapter 4

Final circuit design

This chapter describes the exact design of the final circuit. First, the used components are described in some detail. Then, a schematic with all components is given, together with an explanation for the used components. Finally, some drawings shows the implementation of the circuit is the STM.

4.1 PCB components

The resistors and capacitors used are SMD 0805 or 0603 components. Capacitors are labelled NP0 meaning they vary only 0.5% between -55 to +125 degrees centigrade.

The transistors are HEMTs developed by Dong et al. [13]. They show good noise characteristics of $2.2\text{fA}/\sqrt{\text{Hz}}$ at 1MHz and $0.26\text{nV}/\sqrt{\text{Hz}}$ at 100kHz (appendix figure C.5, transistor B2). For the MHz range, the voltage noise is expected to be slightly smaller, to $0.2\text{nV}/\sqrt{\text{Hz}}$, because of the $1/f$ behaviour. Details are described in appendix C.

In the first generation amplifier, the circuit board was make from Rogers TMM10i. This because of its low outgassing properties. The circuit board in the amplifier proposed by this report uses Rogers 4003. The Rogers 4003 has a dielectric constant of 3.38, while TMM10 has 9.20. Thermal conductivity of 0.76 for TMM10i and 0.71 for 4003. Based on these specifications, no changes are expected between the amplifier from Bastiaan et al. [1] and the proposed one. *

The inductor consists of niobium wire. Important is that the wire has

*Data is obtained from companies official website www.rogerscorp.com .

no normal metal coating, as this would reduce the Q-factor significantly [24]. The core is made out of Macor, as this also causes little dissipation of RF field induced by the coil. Last, the coil is shielded using niobium. The implemented coil is shown in appendix C and figure 4.4.

4.2 Circuit design

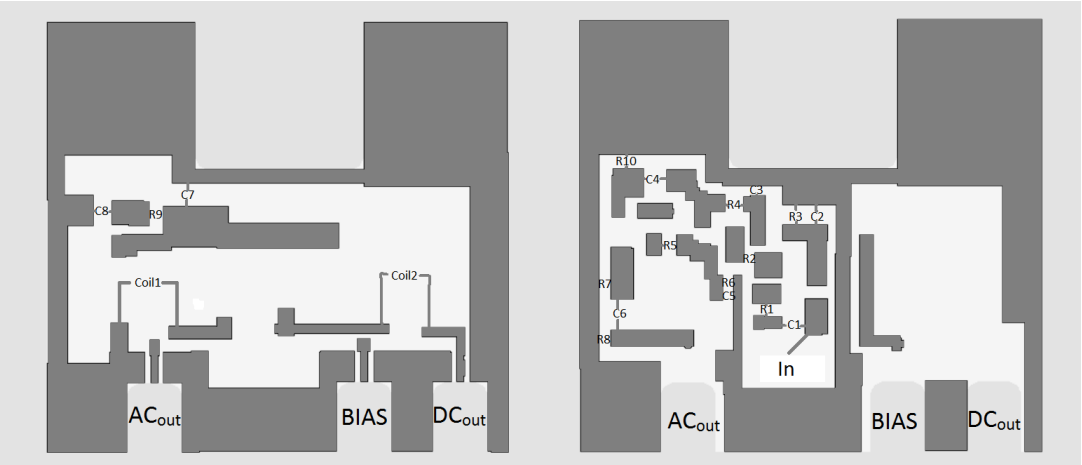

Figure 4.1: *Schematic with all components as is shown in table 4.1. The right hand side faces the STM.*

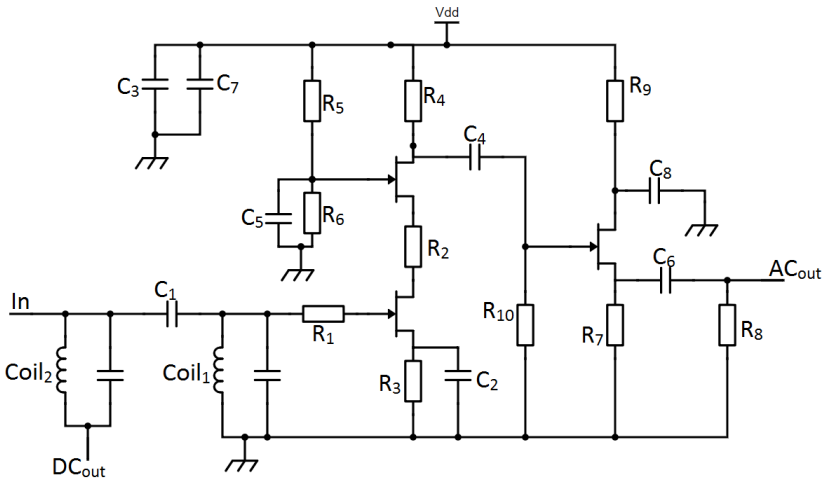

Figure 4.2: *Schematic circuit of figure 4.1.*

A schematic of the physical circuit is given by figure 4.1. The circuit diagram is given in figure 4.2 with all elements denoted in table 4.1. Capacitors C_{2-8} only have the purpose of blocking DC signal while acting as short for high frequency signal. Reistors R_1 and R_2 have no function in the circuit, they only dampen out high frequency (>100MHz) oscillations. Some elements require special attention.

Table 4.1: *Circuit elements as shown in figures 4.1 and 4.2.*

C1	100pF
C2,C3,C4,C5,C6,C7,C8	220nF
R1,R2	10Ω
R3	130Ω
R4	2kΩ
R5	1MΩ
R6	68kΩ
R7	200Ω
R8	68Ω
R9	2.2kΩ
R10	3kΩ

4.2.1 Common Source biasing; R_3,R_4

First of all, the source resistor of the CS transistor, R_3 (first stage). The resistance is set to be 130Ω. From figure C.6, transistor B2 in appendix C, the drain source current is I_{DS} =0.5mA for a bias gate-source voltage of $V_{GS} = -78.7$mV. This would correspond to a resistance of $R_S \approx 160\Omega$. This resistance is chosen slightly smaller, such that the current is slightly larger and the transconductance is larger. The transconductance should be about 30-35 mS.

The drain resistance of the CG transistor, R_4 is set to 2kΩ. If this is too small, the gain is too small. However, if it is too large, the dissipation is too large.

The bias voltage is determined by the above mentioned parameters, according to $V_{DS} = I_{DS}(R_2 + R_3 + R_4) + V_{DS,CG} + V_{DS,CS}$, where $V_{DS,CG}$ and $V_{DS,CS}$ are both 100mV for optimal noise performance.

4.2.2 Common Drain biasing; R_7, R_9, R_{10}

The source resistance of the third transistor, R_7 is set at 200Ω. From figure C.7, transistor A1, the drain-source current of transistor is set at $I_{DS,CD}$=0.5mA.

This required a gate-source voltage of about 100mV, hence the 200Ω resistor. Resistor R_9 is determined by the bias voltage i.e. $R_9 = \frac{V_{bias}-V_{DS}}{I} - R_7$. The total dissipation can be written as

$$P = I_{DS,CS}^2(R_2+R_3+R_4) + I_{DS,CD}^2(R_7+R_9) + I_{DS,CS}(V_{DS,CS}+V_{DS,CG}) + I_{DS,CD}V_{DC,CD}. \tag{4.1}$$

This is approximately equal to 2mW. The resistance R_{10} set the gate voltage at 0V. This is chosen to be large, such that the gain of the CG is large.

4.2.3 Common Gate biasing; R_5,R_6

This voltage divider determines gate voltage of the CG. If this value where too small, e.g. grounded, the gate-source voltage would be too small and thus the noise is too large. It is important to have the CG in saturation, which is why a voltage divider of $\beta \approx \frac{68k\Omega}{68k\Omega+1000k\Omega}$ is chosen. The bias voltage will be slightly larger than V_{Bias}=80mV+100mV+100mV+1000mV=1.28V. The voltage at the gate is thus slightly larger than 80mV. The gate-source voltage of the CG is thus sligthly smaller than 100mV. So the transistor is well in saturation.

4.2.4 Impedance matching; R_7,R_8

The output should match the 50Ω of the coaxial cable. This thus requires R_8 to be 68Ω, such that the output is $R_{out} = \frac{R_7R_8}{R_7+R_8} \approx 50\Omega$.

4.3 Implementation in STM

The limited space has determined the shape of the circuit as shown in figure 4.1. The implementation of this circuit is shown in figure 4.3. The circuit is attached to the side poles using four clamps. From figure 4.4 one can see that the clamps are not symmetrically spaced. This is due to the location of PCB components. Besides attachment, the clamps also have the purpose of thermalisation.

Three connectors are shown in figure 4.3, which correspond to 'DC OUT', 'BIAS' and 'AC OUT' from figure 4.1. The 'In' is visible in figure 4.5. This is directly connected to the STM, such that the input capacitance is small.

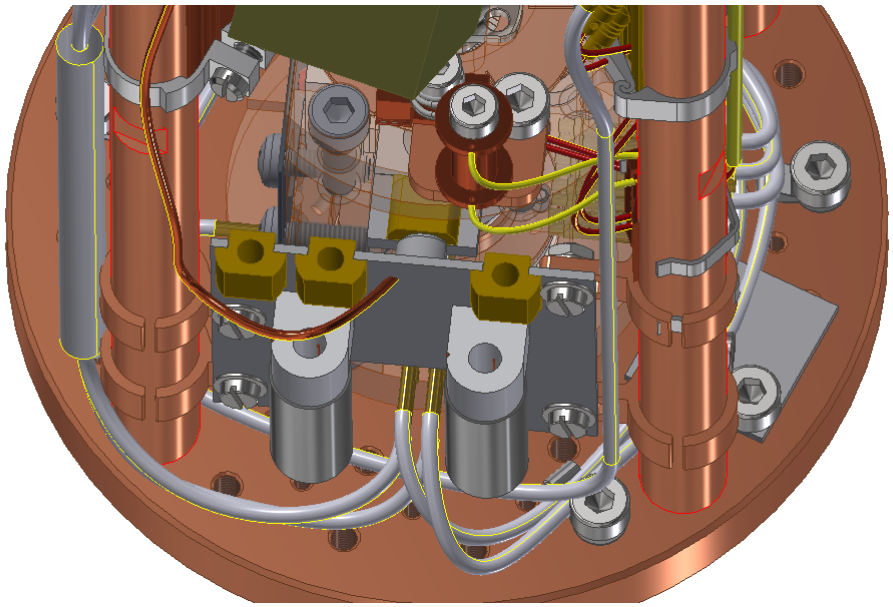

Figure 4.3: *Implementation of the PCB with attachment. The clamps to the poles have the function of both attachment and thermalisation.*

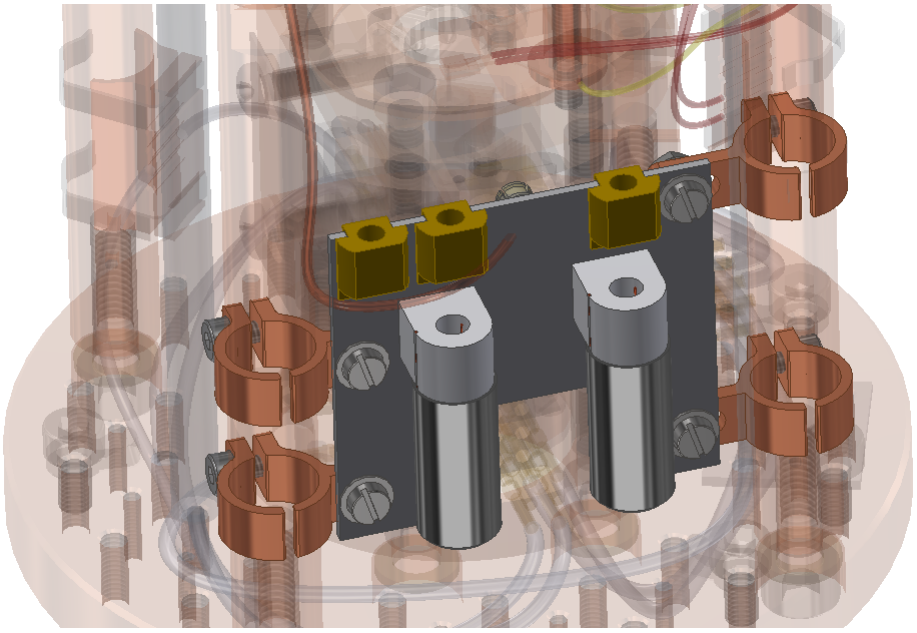

Figure 4.4: *Front of the PCB. The two inductors with their shielding are visible.*

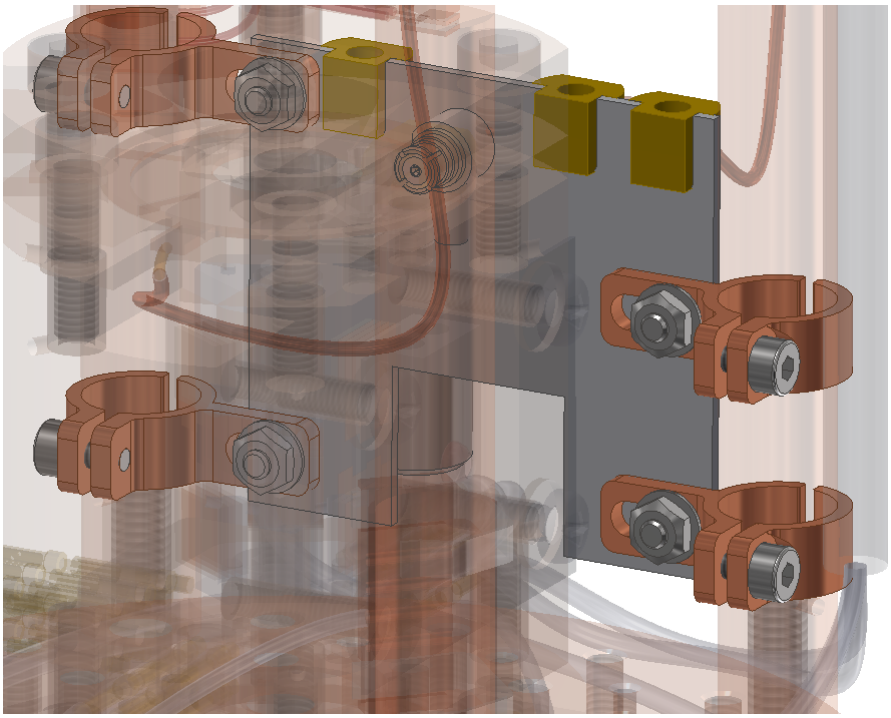

Figure 4.5: *The back of the PCB. The connector perpendicular to the PCB is the input.*

Chapter 5

Results and discussion

This section shows all test circuits, i.e. the room temperature measurements. First, the results of cascoding are presented. The benefit of cascoding as well as some points of concern are explained. Then, the results of bootstrapping are presented. This turned out to be unsuccessful and possible explanations are given.

5.1 Cascoding

The reduction of the miller capacitance is measured using a LC resonator at the input. All measurements have a 33μH input coil with an effective parralel capacitance of 1.6pF. The other parasitic capacitances (transistor, cable) are included in this effective capacitance. The Self Resonance Frequency (SRF) is then 22 MHz.

5.1.1 Not cascoding

To show the relevance of cascoding, first the shift in resonance frequency is given for a single CS transistor, as is shown in figure 5.2. In therms of voltages, $S_{21} = 20\log(\frac{v_{in}}{v_{out}})$. The units of this parameter are arbitrary, but they can be viewed as a measure of the impedance of the resonator. The increase of bias voltage corresponds to a larger gain and therefore with a larger miller capacitance. The equivalent circuit is shown in figure 5.1.

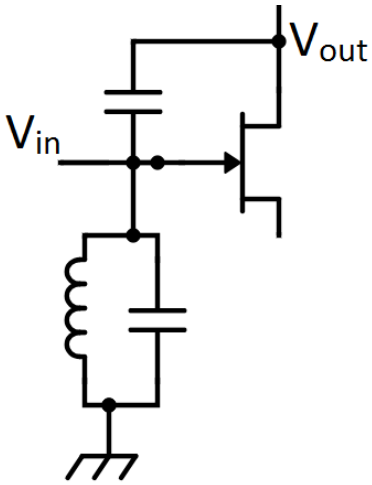

Figure 5.1: *Schematic of the used circuit. The capacitance between the gate and the drain is effectively enlarged, as visualised in figure 5.2.*

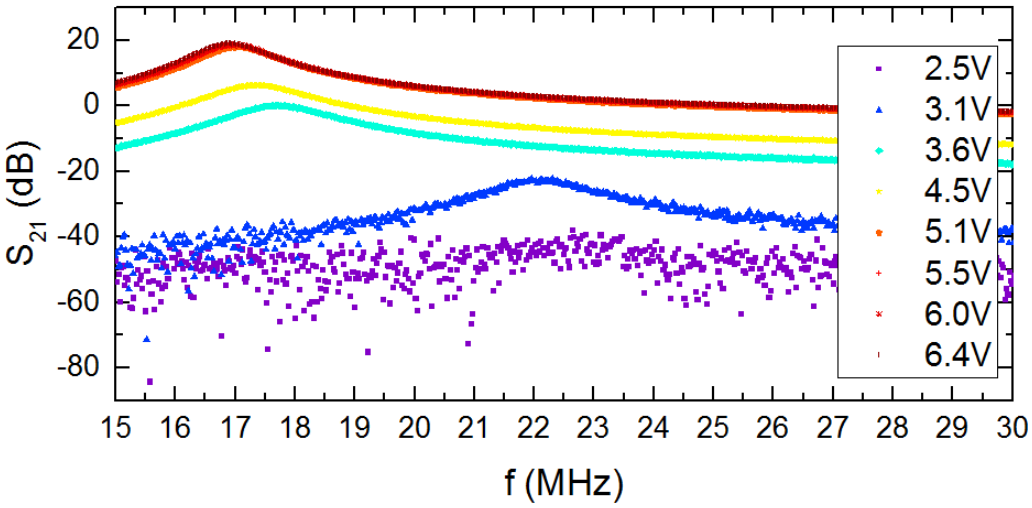

Figure 5.2: *If the first stage is not cascoded, the resonance frequency would shift due the increasing gain. The gain scales with bias voltage (legend) over the transistor.*

The vertical axis in figure 5.2 is the ratio between the out- and input voltage. This is proportional to the impedance of the resonator. The number do not provide much information about the resonator, because the gain is also varied (the tails of the resonator also move up). Most important is

that the frequency changes as a function of the bias voltage, or equivalently, the frequency changes as a function of the gain in the tails.

Using the relation $\frac{\Delta C}{C} = \frac{f_0^2 - f^2}{f^2}$, the miller capacitance ΔC can be calculated. The resonance frequency in figure 5.2 decreases from 22Mhz to 17Mhz and with a capacitance of the coil of about 1.6pF, the miller capacitance is 1.1pF. Together with the flat V/V gain of 10, the gate-drain capacitance can be estimated to be 0.1pF. Note the for the low-noise HEMTs, the gate-drain capacitance is 1pF, and the miller effect becomes more substantial.

5.1.2 Cascoding applied

Now that the increase in effective capacitance is clear, the effect of cascoding can be shown. It is important to have the cascaded transistor (CG) to be in saturation. This can be controlled by two resistors which voltage divider V_{DD}. Figure 5.3 shows this setup, where R_{top} and R_{bottom} determine the gate voltage using $V_{gate} = V_{DD} \frac{R_{bottom}}{R_{bottom} + R_{top}}$. Figure 5.4 shows the cascoding effect for a voltage dividing ratio of 1/3.

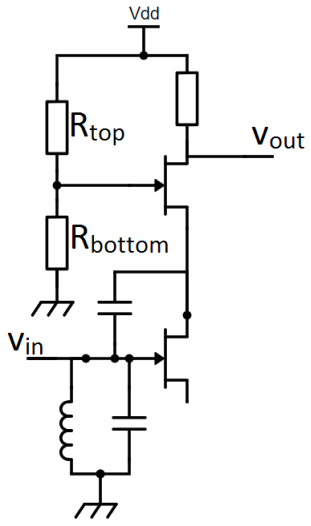

Figure 5.3: *The equivalent circuit of cascoding is given. The resistors R_{top} and R_{bottom} form a voltage divider, which determine the saturation point of the cascaded CG transistor.*

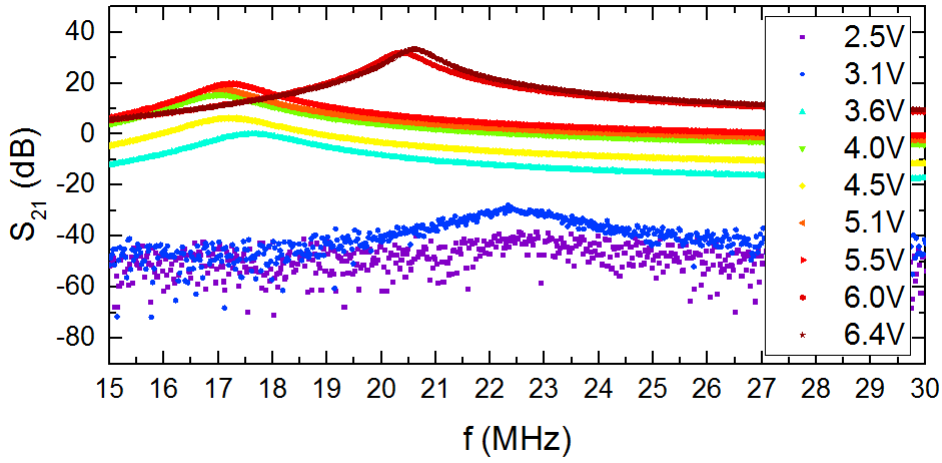

Figure 5.4: *Cascoding effect for a top resistor of 10kΩ and a bottom resistor of 20kΩ. The gate voltage is large, so the CG saturates only for high bias voltages, hence the resonance frequency shift back up. The legend indicates the bias voltage.*

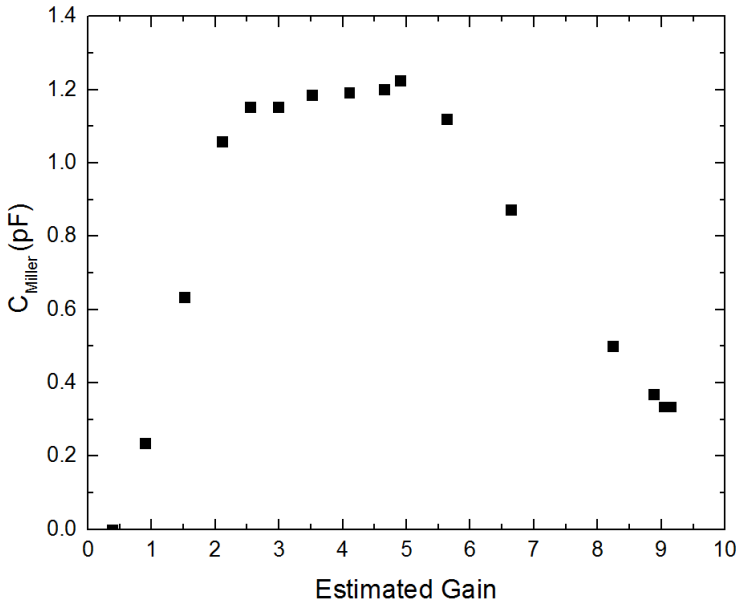

Figure 5.5: *An estimate of the miller capacitance is set against a rough estimate of the gain for voltage dividing ratio $\frac{10k\Omega}{10k\Omega+39k\Omega}$. This plot is just qualitative. First, gain increases fast giving larger miller capacitance. The second transistor just acts as a resistor of about 1kΩ when not in saturation. At the downward slope, the cascaded transistor becomes saturated and thus the miller capacitance goes down.*

For larger bias voltages, i.e. larger gains, the resonance frequency first goes down, but goes up again at some point. Converting this resonance frequency to capacitances, one can more clearly see the effect of cascoding, as is shown in figure 5.5.

5.1.3 Optimal bias voltage

The ratio of voltage dividing is crucial since the gate voltage determines when the CG transistor is in saturation.

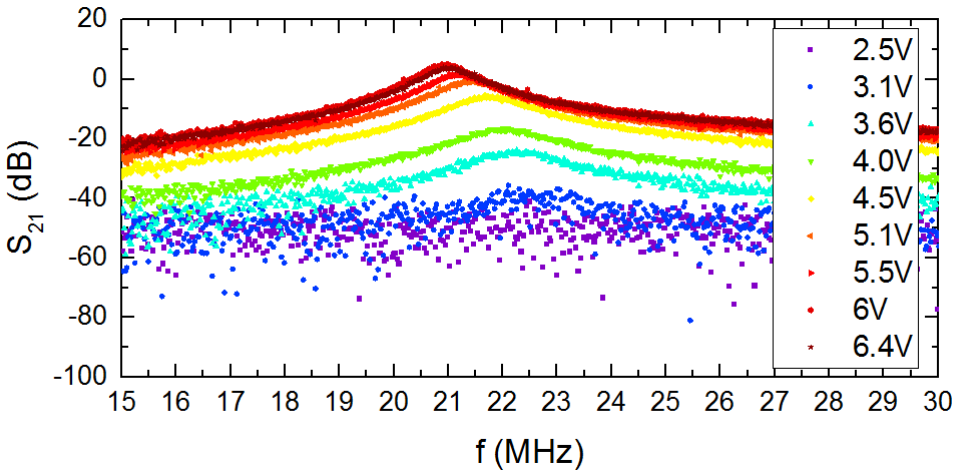

Figure 5.6: *Cascoding effect for a top resistor of 10kΩ and a bottom resistor of 1MΩ. The gate voltage is small, so the CG saturates rapidly.*

If the gate voltage is too small, as shown in figure 5.6, the miller effect is not visible, but drain source voltage of the CG stage (cascaded stage) is too large, which leads to a worse noise performance for the HEMTs. If the gate voltage is too large, the CG saturates for large bias voltages. For these large bias voltages, the CS (first transistor) has a too large drain-source voltage, which also gives a worse noise performance. The optimal form is the intermediate voltage divider as is given by figure 5.7. Here the shift in resonance frequency only happened at one bias voltage.

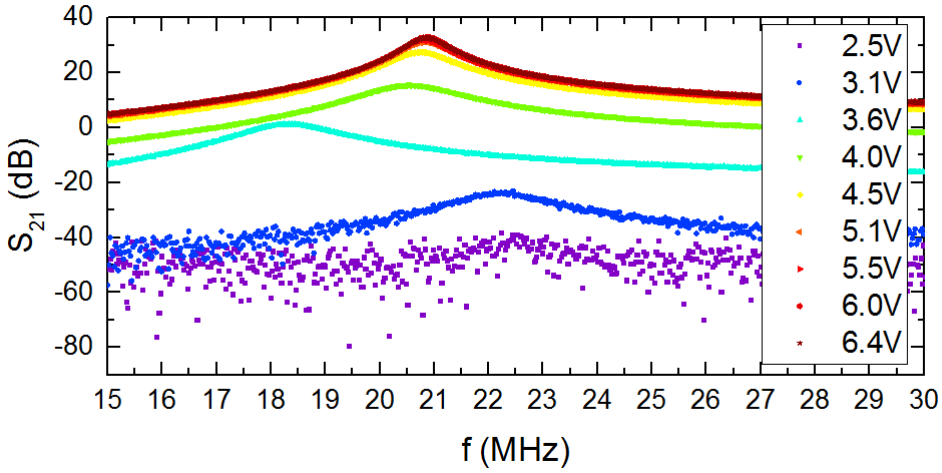

Figure 5.7: *Cascoding effect for a top resistor of 10kΩ and a bottom resistor of 100kΩ. This ratio is between those of figures 5.6 and 5.4. Only at 3.6V bias voltage, the miller effect is apparent.*

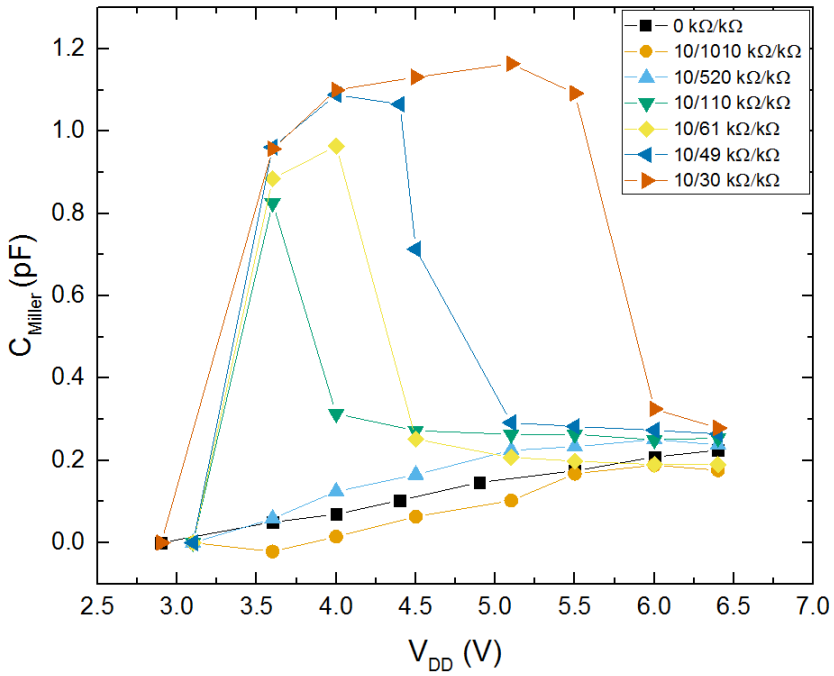

Figure 5.8: *33µH inductor, no additional capacitance. The resistance ratio is the voltage division ratio, i.e. the fraction of V_{DD} at the gate fo the CG transistor. For a too large voltage dividing ratio, the gate voltage is too large and the bootstrapping has no effect.*

Figure 5.8 shows this relation even more clearly. The ideal situation would be exactly the voltage dividing ratio of $\frac{10k\Omega}{10k\Omega+110k\Omega}$, i.e. a top resistor of 10kΩ and a bottom resistor of 100kΩ. Actually, the voltage dividing ratio should be slightly more than 10/110 to achieve optimal performance.

5.2 Bootstrapping

In contrast to the idea of cascoding, bootstrapping does not show good results, and is therefore not implemented in the final amplifier. It is still interesting to review its functioning and instabilities.

5.2.1 Bootstrapping applied

Bootstrapping requires a non-inverting constant amplifier, which is a flat gain and a phase shift around zero. This is measured by disconnecting the bootstrapping capacitor C_{bt}, the setup is shown in 5.9. Figures 5.10 shows a flat gain and flat phase response, so that indeed a non-inverting amplifier is created.

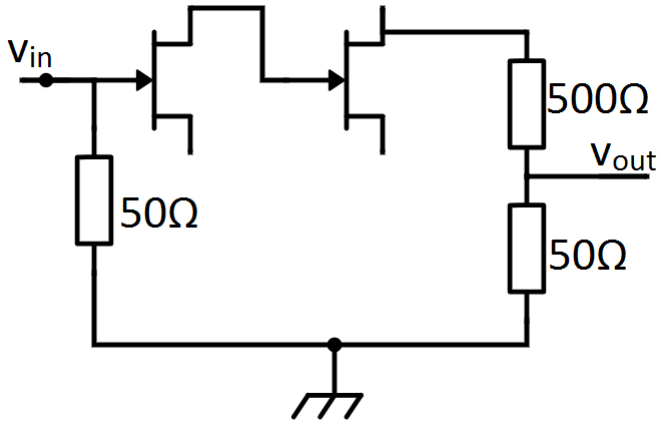

Figure 5.9: *Circuit for measuring flat gain. The input and output resistances are 50Ω. The output is voltage divided, such that the signal is attenuated by approximately 20 dB. This should be corrected for in figure 5.10.*

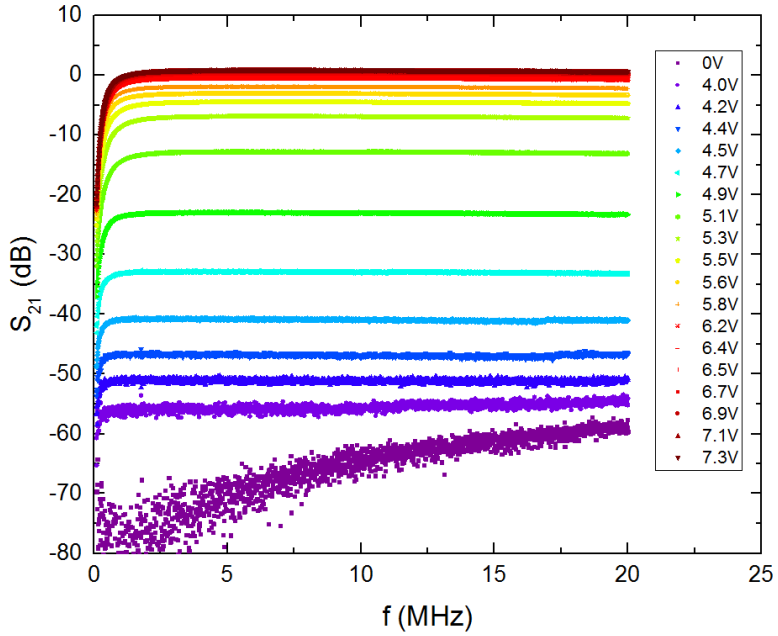

Figure 5.10: *Gain of the amplifier. One should correct for the 20dB attenuation by adding 20dB. The amplitude gain goes up to 10V/V.*

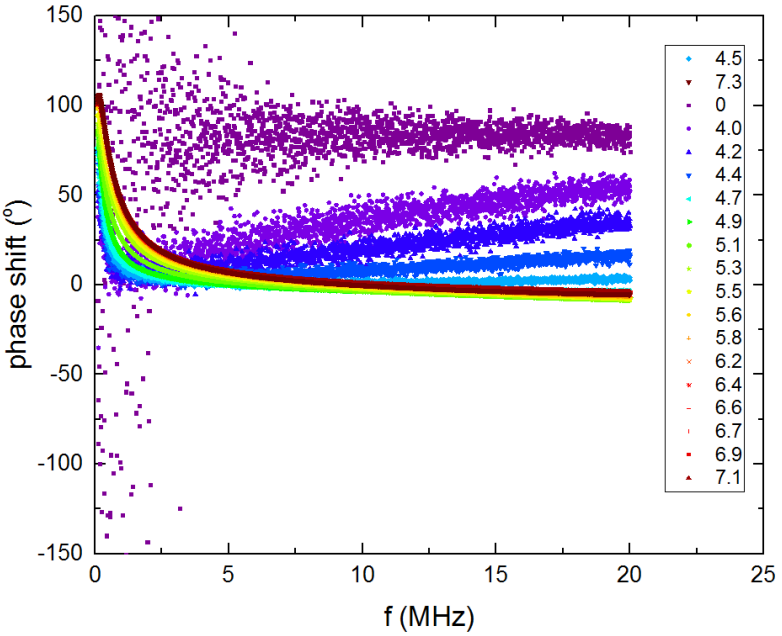

Figure 5.11: *The phase of the transmitted signal. The phase shift is approximately zero.*

The effect of bootstrapping is the opposite of cascoding. A 33μH inductor is connected in parallel with a total capacitance of 63pF. When increasing the bias current, the gain increases and thus the effective capacitance decreases. Figure 5.12 shows the increase in resonance frequency with increasing gain.

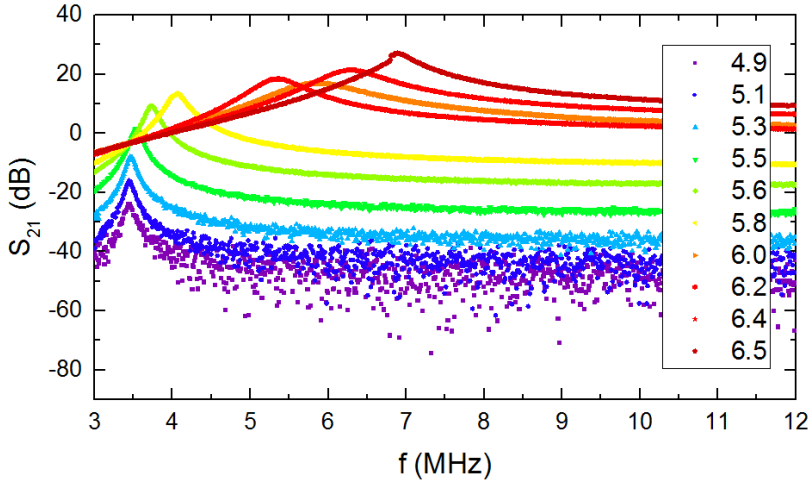

Figure 5.12: *Shift in resonance frequency after bootstrapping. The resonance frequency doubles due to the effect of bootstrapping.*

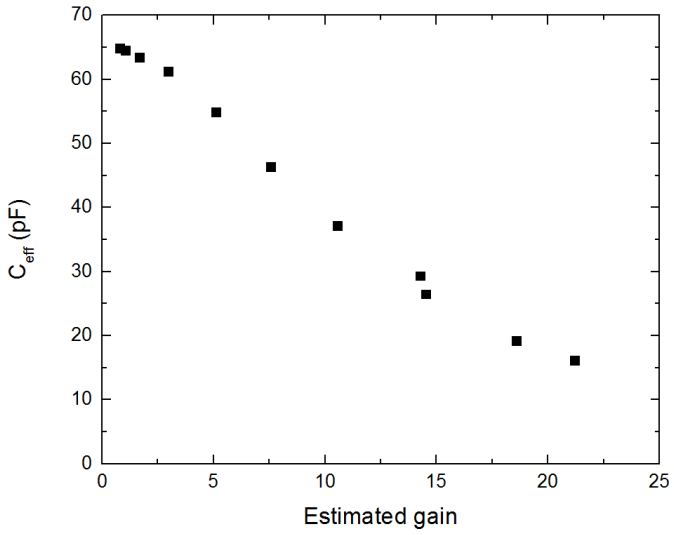

Figure 5.13: *Estimate of the effective parallel capacitance as a function of the estimated amplitude gain. Again, the gain is a rough estimate.*

The capacitance is effectively reduced to 16pF. Thus, the resonance frequency can effectively be doubled, which thus significantly extends the bandwidth. The effective capacitance as a function of gain is given in figure 5.13.

5.2.2 Instability

Figure 5.12 shows a good functioning of the LC resonator. However, in practise, some instability occurs. First of all, when applying a too large V_{DD}, i.e. the gain is too large some 'strange' peaks occur. These peaks are given in figure 5.14. From a certain drain voltage, the peak becomes sharp and higher harmonics occur. This peak in unpredictable (shifts in resonance frequency) and should therefore not be used for measurements.

The instability shows peaks at the higher harmonics of resonance frequency as figure 5.15 shows. Also, when the bootstrapping capacitance is increased, the instability occurs. Also the peak of the instability shifts down as is shown in figure 5.16.

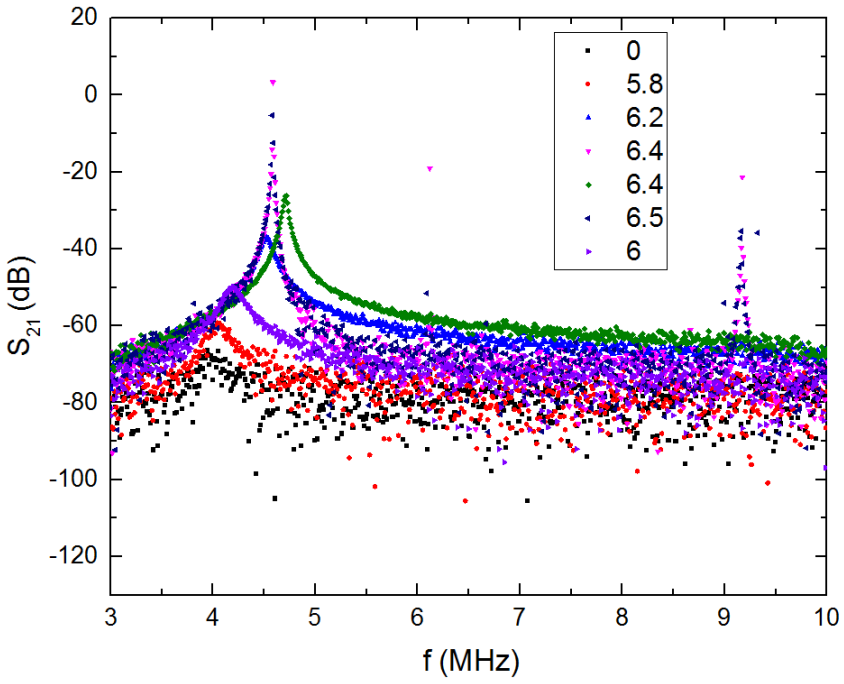

Figure 5.14: *If unstable, peaks become much sharper compared to usual LC resonance impedance. Also for equal bias voltage (6.4V) and thus equal gain, the peak can be stable or unstable.*

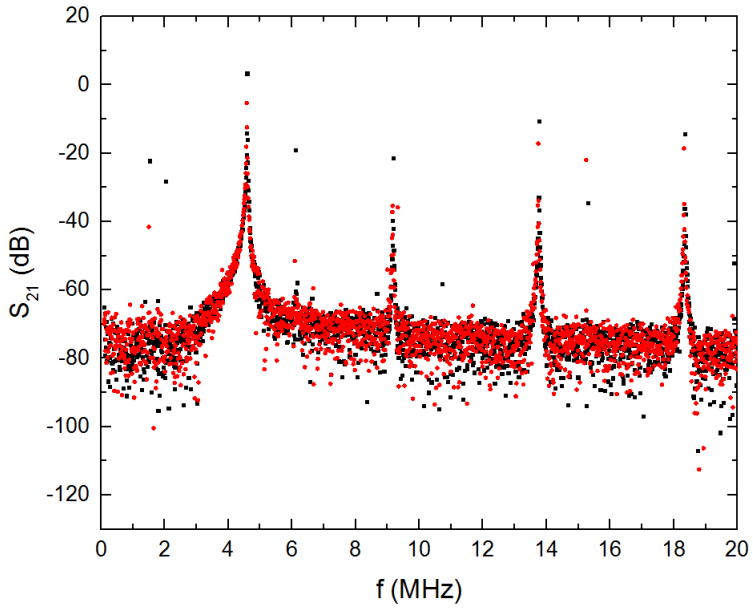

Figure 5.15: *The main frequency peaks are at $f = f_0 n, n \in \mathbb{N}$. There are also peaks at $f = \frac{5}{4} f_0$ visible, which correspond to higher harmonics.*

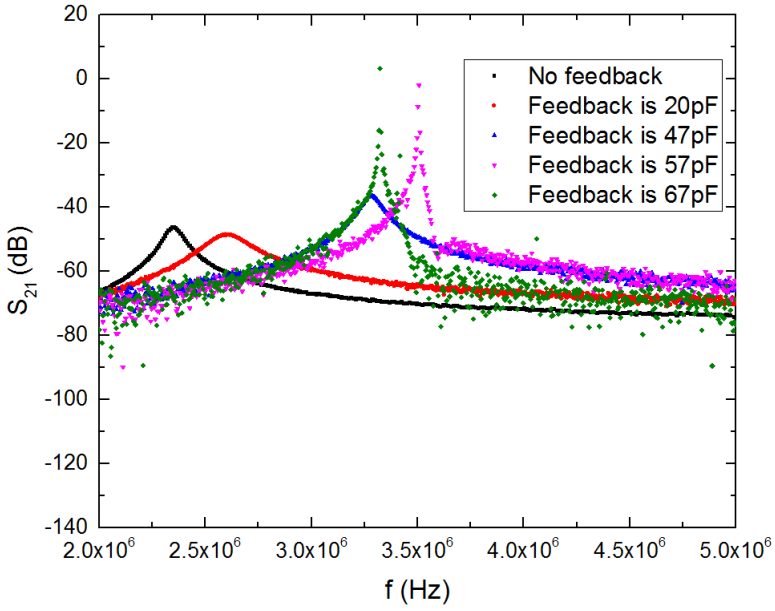

Figure 5.16: *33μH input inductance, 130 pF parallel capacitance. For too large capacitance, the LC resonance becomes unstable.*

5.2.3 Possible explanations

An explanation for the instability is that the input power on the transistor is too large. The transistor gives unpredictable behaviour and only transmits some signal around the frequency where the signal is maximal. However,the input power has been attenuated significantly using a tunnelling resistor and RC filters. This did not influence the instability.

A second explanation is based on section 2.2.2. Reducing the capacitance is the same as reducing the mass. This is a difficult to visualise, but the equation could also be mapped to a pendulum with two masses at two different lengths

$$\ddot{\theta} + g\frac{m_1 l_1 + m_2 l_2}{m_1 l_1^2 + m_2 l_2^2}\theta = 0. \tag{5.1}$$

Note that if one mass reaches above turning point, a negative contribution is added, i.e. the pendulum is bootstrapped. Having two masses above and below the turning point is intuitively unstable. However, mathematically, only if $m_1 l_1 + m_2 l_2 < 0$, the pendulum is unstable. This means that one would reach infinite frequency before becoming unstable. Although this does not explain the instability, it does give an intuitive idea. Any imperfections (e.g. gain or phase depend on input signal) would create an unstable system. However, from figures 5.10 and 5.11, the phase and gain both seem flat.

A third explanation is that the amplifier forms a oscillator. The transfer function from the output of the amplifier to the input of the amplifier is given by

$$H(\omega) = A\frac{-\omega^2 L C_{bt}}{1 - \omega^2 L(C + C_{bt})} \tag{5.2}$$

where an infinite Q-factor is considered for simplicity. Note that the input voltage is ”unknown” in the above equation. If this is considered to be ”known”, as it should, the circuit is stable (see equation 3.6). Equation 5.2 suggests that the gain is largest at $f = \frac{1}{2\pi}\frac{1}{\sqrt{L(C+C_{bt})}}$. Also there is no phase shift around this frequency (also required for oscillations, see section 2.5). This suggests that the resonance frequency goes down with increasing capacitance, which is consistent with figure 5.16. However, if this explanation was correct, the bootstrapping would not have worked at all. Besides, the Barkhausen theorem would have been satisfied long before.

This explanation can be tested by high pass filtering the lower frequency. However, using low order filters, only artefacts of this filter can be shown. If the filters frequency is too high, the full signal is attenuated

such that the total gain is less than one and the bootstrapping is pointless. If the filter has a too low cut-off frequency, the instabilities still occur.

Chapter 6

Cryogenic measurements

Unfortunately, the final transistor is still under construction, so no data can be displayed here.

6.1 Gain measurement

To measure the gain, the input and output are connected to 50Ω. The Vector Network Analyser (VNA) measures the power amplification in those lines. The figure to be inserted would show a flat voltage gain of approximately 22 up to about 20MHz.

6.2 LC resonator

To measure the LC-resonator, a 50Ω is again connected to the output, but the input consists of the two coils with their coupling capacitor, just as is indicated in figures 4.2. If the input also has a small capacitance connected to it, the resonance frequency and bandwidth can be measured, from which the inductance is measured.

The total input noise can be measured using a Lock-In at the output and no input signal. The signal at the resonance is predominantly caused by current noise. The noise floor is due to the voltage noise.

6.3 Noise estimations

Because of the lack of experimental data, some estimations are made. The estimated voltage noise is $0.2\text{nV}/\sqrt{\text{Hz}}$, which is only due to the transis-

tor voltage noise. The total current noise is the sum of the noise of the two coils and the transistor. This is estimated using $S = \sqrt{2\frac{4k_bT}{Q\omega_0 L} + (2.2 \cdot 10^{-15})^2}$. For $Q = 600$, $\omega_0 = 5$MHz and $L = 66\mu$H, the input current noise is about $19\text{fA}/\sqrt{\text{Hz}}$.

Chapter 7

Conclusion and outlook

In order to improve the bandwidth, one should measure the bandwidth of the SNR instead of the bandwidth of the impedance. The bandwidth of the SNR can be improved by increasing the gain, such that the white voltage noise sources after the resonator have a smaller influence. In the amplifier an amplitude gain of 22 is chosen. Because of the Miller effect, this would add a capacitance of 22pF, which reduces the bandwidth. This can be prohibited by using cascoding which is a CS transistor followed by a CG transistor. In order to match the 50Ω of the coax cable, the CG is followed by a CD with an output resistance of 50Ω and unity gain.

This setup would give an input current noise of $19\text{fA}/\sqrt{\text{Hz}}$ and a voltage noise of $0.2\text{nV}/\sqrt{\text{Hz}}$.

Reducing the capacitance with bootstrapping, i.e. a feedforward signal through a transistor, would improve the SNR even more. In the testing stage, this shows instabilities which are not fully understood. The best explanation is given by the Barkhausen oscillation theorem; for a gain larger than one and no phase shift oscillations will occur.

7.1 Outlook

This project has focused mainly of the transistor stages an less on the inductor. Improvements might be achieved by fabrication a coil with higher Q-factor as was reported in [18][24][25]. The challenge here is to fabricate coils and shielding for a small space and Ultra High Vacuum.

Also a SQUID might be used. For state of the art SQUID current sensors [26] the input current is about $0.08\text{pA}/\sqrt{\text{Hz}}$, which is only one order of magnitude larger. Experimental data show this is possible up to

100kHz. With proper shielding, this should work for higher frequencies as well, such that a good resolution for a large bandwidth can be achieved.

Finally, bootstrapping can still be successful. Using a high order filter to filter out the parasitic oscillations, but leave the effective LC resonance frequency unchanged, the bootstrapping might work. However, there is a trade-off between the bootstrapping capacitor and the order of the filter. To get a small extra noise from the bootstrapping, the capacitance should be small and the order of the filter should be very large. It is unlikely that this would work in practise.

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Appendix A

Derivations

A.1 Electrical noise from scattering picture

In this section, the thermal and shot noise formulas are derived from the scattering picture. Two electrodes are considered with some system in between. In the derivation, Blanter et al. [27] is followed closely. Consider the left electrode with forward moving electrons, created by $a^\dagger_{L,n}$ and backward moving electrons, created by $b^\dagger_{L,n}$, where L stands for "left electrode" and n indicates orbital n. Assuming constant velocity of electrons, the total current is given by

$$I_L(t) = \frac{e}{h}\sum_n \int dE dE' \exp\left[i\frac{E-E}{\hbar}\right][a^\dagger_{L,n}(E)a_{L,n}(E') - b^\dagger_{L,n}(E)b_{L,n}(E')], \tag{A.1}$$

which is easily understood as the number of right moving minus the number of left moving electrons.

The next step is to relate the right moving electrons to the left moving electrons

$$b_{\alpha,m}(E) = \sum_{\beta,n} s_{\alpha,\beta;m,n}(E)a_{\beta,n}(E) \tag{A.2}$$

where the diagonal elements, i.e. $s_{\alpha,\alpha;m,n}$ form the reflections and the off diagonal element the transmission.

Assuming a Fermi-Dirac distribution, the time averaged current is given by

$$\langle I\rangle = \frac{e}{h}\sum_{m,n}\int dE s^\dagger_{LR;m,n}s_{LR;n,m}[f_L(E) - f_R(E)] \tag{A.3}$$

where $1 - s^\dagger_{LL}s_{LL} = s_{RL}$ is used. $f(E)$ is the Fermi-Dirac distribution. One

can now define

$$G = \frac{e^2}{h} \sum_{m,n} s^{\dagger}_{LR;m,n} s_{LR;n,m} = \frac{e^2}{h} \sum_n T_n \tag{A.4}$$

where in the last line, T_n repesents the sum of squired of eigenvalues of $s_{LR,mn}$.

In order to find the noise power, one can define a noise power given by

$$P(t - t') = \frac{1}{2} \langle \Delta I(t) \Delta I(t') + \Delta I(t') \Delta I(t) \rangle, \tag{A.5}$$

where $\Delta I(t) = I(t) - \langle I \rangle$. The fourier transform is

$$2\pi\delta(\omega - \omega') P(\omega - \omega') = \langle \Delta I(\omega) \Delta I(\omega') + \Delta I(\omega') \Delta I(\omega) \rangle. \tag{A.6}$$

Filling in equation A.1 the noise power is
$P(\omega) = \frac{e^2}{h} \sum_{\alpha\beta} \sum_{mn} \int dE (\delta_{\alpha,L;\beta,L;m,n} - s^{\dagger}_{L,\alpha;m,k} s_{L,\beta;n,k})(\delta_{\alpha,L;\beta,L;m,n} - s^{\dagger}_{L,\beta;n,k} s_{L,\alpha;m,k})$
$(f_\alpha(E)[1 - f_\beta(E + \hbar\omega)] + [1 - f_\beta(E)] f_\beta(E + \hbar\omega)$.
Summing over L and R and converting the $s_{\alpha\beta,mn}$ into eigenvalues, the power spectrum is

$$P = \frac{2e^2}{h} \sum_n \int dE [T_n (f_L(1 - f_L) + f_R(1 - f_R)) + T_n(1 - T_n)(f_L - f_R)^2]. \tag{A.7}$$

After performing the intergration, the spectrum is

$$P = \frac{2e^2}{h} [2k_b T \sum_n T_n^2] + eV \coth(\frac{eV}{2k_b T}) \sum_n T_n(1 - T_n)]. \tag{A.8}$$

Using $G = \frac{e^2}{h} \sum_n T_n$, the first therm on the RHS in the above equation is the thermal noise

$$P_{th} = 4k_b T G \tag{A.9}$$

and the second therm on the RHS is the shot noise. For small tunnelling junction, as is the case with STM, the shot noise is

$$P_{SN} = 2eVG = 2e\langle I \rangle. \tag{A.10}$$

In the derivation, no distinction has been made between tunnelling barriers and materials in the barrier. The point is that the tunnelling barrier also contributes to the thermal noise. However, a tunnelling barrier is typically of the order of 1GΩ, while the resonator has a maximum impedance of 1MΩ, so the current noise from the tunnelling junction is much smaller. When the tunnelling barrier impedance is comparable with the resonator, it is of importance.

A.2 Thermal noise inductor

The noise of any electrical element is given by its dissipative elements. Therefore, one could immediately determine the voltage noise of an inductor;

$$S_V = 4k_bT\Re[Z_{LC}] = 4k_bT|Z_{LC}|^2\frac{R}{\omega^2L^2+R^2} \tag{A.11}$$

and thus, effectively the current noise is approximately given by

$$S_I = \frac{4k_bT}{Q\omega L}. \tag{A.12}$$

An alternative way of deriving the thermal noise is by considering the circuit in figure 2.2. The resistor produces a thermal noise given by $S_I = \frac{4k_bT}{R}$. Analysing this circuit gives

$$V_1 = \sqrt{S_I}\frac{R(j\omega L+Z'}{R+j\omega L+Z')} \tag{A.13}$$

and

$$V_2 = V_1\frac{Z'}{j\omega L+Z'} = \sqrt{S_I}\frac{RZ'}{R+j\omega L+Z'} = \sqrt{S_I}\frac{R}{\frac{R+j\omega L}{Z'}+1}. \tag{A.14}$$

Note that the total impedance is given by

$$Z^{-1} = Z'^{-1} + (j\omega L+R)^{-1}. \tag{A.15}$$

So V_2 can be simplified to

$$V_2 = \sqrt{S_I}\frac{RZ}{R+j\omega L} \tag{A.16}$$

so the noise power at V_2 is

$$S_{V_2} = \frac{4k_bT}{R}\frac{R^2|Z|^2}{\omega^2L^2+R^2} = 4k_bT|Z_{LC}|^2\frac{R}{\omega^2L^2+R^2} \tag{A.17}$$

which is indeed equal to A.11.

A.3 Proper bandwidth definition

The proper definition of the bandwidth is given by equating the impedance of the LC-resonator to the optimal noise impedance $\sqrt{\frac{S_V}{S_I}} \equiv \tilde{Z}$. So the equation to solve is $Z_{LC} = \tilde{Z}$. This equation is

$$|j\omega C - \frac{j\omega L}{\omega^2 L^2 + R^2} + \frac{R}{\omega^2 L^2 + R^2}| = |\frac{1}{\tilde{Z}|}. \tag{A.18}$$

For simplicity, the denominators can be approximated as $\omega^2 L^2 + R^2 \approx= \omega^2 L^2$. Furthermore, one can use $Q = \frac{\omega L}{R}$, so

$$(C\omega - \frac{1}{\omega L})^2 + \frac{1}{(Q\omega L)^2} - \frac{1}{\tilde{Z}^2} = 0, \tag{A.19}$$

$$\omega^4 - \omega^2(\frac{2}{LC} + \frac{1}{(\tilde{Z}C)^2}) + \frac{1}{Q^2(LC)^2} + \frac{1}{(LC)^2} = 0. \tag{A.20}$$

Which have solutions

$$\omega^2 = \frac{1}{LC} + \frac{1}{2(\tilde{Z}R)^2} \pm \sqrt{(\frac{1}{LC} + \frac{1}{2(\tilde{Z}R)^2})^2 - \frac{1}{Q^2(LC)^2} - \frac{1}{(LC)^2}}, \tag{A.21}$$

$$\omega^2 = \frac{1}{LC} + \frac{1}{2(\tilde{Z}R)^2} \pm \sqrt{(\frac{1}{\tilde{Z}C)^2 LC} + \frac{1}{4(\tilde{Z}C)^4} - \frac{1}{Q^2(LC)^2}}. \tag{A.22}$$

This is approximately

$$\omega = \sqrt{\frac{1}{LC} + \frac{1}{2(\tilde{Z}C)^2}} \pm \frac{1}{2} \frac{\sqrt{(\frac{1}{\tilde{Z}C)^2 LC} + \frac{1}{4(\tilde{Z}R)^4} - \frac{1}{Q^2(LC)^2}}}{\sqrt{\frac{1}{LC} + \frac{1}{2(\tilde{Z}C)^2}}}. \tag{A.23}$$

The bandwidth is than approximately given by

$$BW = \sqrt{\frac{1}{(\tilde{Z}C)^2} - (\Delta\omega)^2}, \tag{A.24}$$

where $\Delta\omega$ is the bandwidth of the resonator.

Version of January 23, 2019– Created January 23, 2019 - 21:23

Appendix B

SQUID current sensor

The figure of merit of a SQUID is given by its energy resolution ϵ given in units $\frac{\mathrm{J}}{\mathrm{Hz}}$. Typically, a SQUID has a resolution of $\epsilon = 100h$ (h is the Planck constant) [26], while state of the art SQUIDs have a resolution below 10h. Definitions can be cumbersome in this case, for clarity, the following definitions are made. An input current noise $S_{I,in}$ in converted into a flux $S_{\Phi,in} = M_{in}^2 S_{I,in}$. Furthermore, there is some noise from the SQUID $S_{\Phi,SQ}$, which can be converted into a current noise $S_{I,SQ} = S_{\Phi,SQ}/M_{in}^2$, where $M_{in} = k\sqrt{L_{in}L_{SQ}}$. The energy resolution is determined by the SQUID noise, i.e. $\epsilon = S_{I,SQ}\frac{L_{in}}{2} = S_{\Phi,SQ}\frac{L_{in}}{2M_{in}^2} = S_{\Phi,SQ}\frac{1}{2L_{SQ}}$.

Following [26], the flux noise is given by $S_{\Phi,SQ}^{1/2} = 4L_{SQ}^{3/4}C^{1/4}\frac{(2k_bT)^{1/2}}{\beta_c}$. Decreasing L_{SQ} would lead to a worse energy resolution, but decreasing the capacitance C leads to a better performance. For a SQUID inductance of 160pH and a input inductance of 2860nH, the input current noise is $65\mathrm{fA}/\sqrt{Hz}$.

This seems worse that the transistor based amplifier, however, it has two advantages. The SQUID is not dependent on frequency. The transistor based amplifier only works in a small bandwidth of the LC resonator. * Furthermore, the SQUID performance is not influenced by decreasing temperatures, while the number of free electrons in the transistors decreases rapidly. Furthermore, the low power goes down quadratically with the temperature [28]. Extrapolating in temperature from 4.2K to 200mK given a current noise of $14\mathrm{fA}/\sqrt{\mathrm{Hz}}$. Note that this extrapolation is not valid, because extrapolating the energy resolution gives $\epsilon = 0.4$, i.e.

*The measurements in [26] go up to 100kHz. There is no sign of degrading behaviour above this frequency, but one can not be sure. High frequency performance can be influence by eddy currents. This can than again be prohibited by proper shielding.

below the quantum limit.

This type of SQUID is commercially fabricated by the company Supracon AG, Jena Germany, where a input current noise of $0.08\text{pA}/\sqrt{Hz}$ is reported. Furthermore, the McCumber parameter is about 0.4-0.5, such that voltage swings over $100\mu\text{V}$ can be observed.

The SNR for the SQUID and HEMT based current sensors are compared in figure B.1.

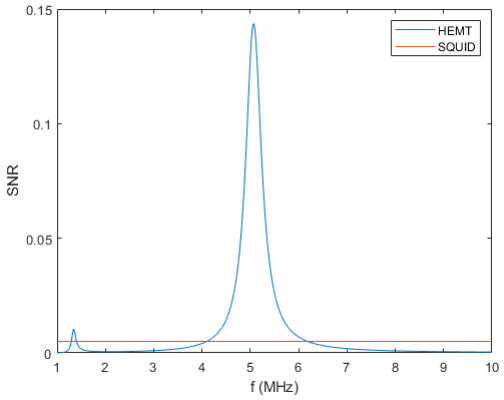


Figure B.1: *The SNR as was shown in figure 3.5. The squid is assumed to have a flat noise of $0.08\text{pA}/\sqrt{Hz}$, where it is assumed that the shielding is perfect, i.e. no noise due to eddy currents. The signal is shot noise, $S = 2|q|I$, for $|q| = e$ and I=100pA.*

Appendix C

Specification sheets

Two types of commerical HEMTs from BROADCOM are used. The data sheet is given below. The most important parameters are the transconductance (g_m) and the noise figure (NF). For the testing, also the maximum input power is important, since this determines the maximum power that can be applied in the VNA.

C.1 ATF34143

ATF-34143 Electrical Specifications

T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameters and Test Conditions			Units	Min.	Typ.[2]	Max.
I_{dss}[1]	Saturated Drain Current		V_{DS} = 1.5 V, V_{GS} = 0 V	mA	90	118	145
V_P[1]	Pinchoff Voltage		V_{DS} = 1.5 V, I_{DS} = 10% of I_{dss}	V	-0.65	-0.5	-0.35
I_d	Quiescent Bias Current		V_{GS} = -0.34 V, V_{DS} = 4 V	mA	—	60	—
g_m[1]	Transconductance		V_{DS} = 1.5 V, $g_m = I_{dss}/V_P$	mmho	180	230	—
I_{GDO}	Gate to Drain Leakage Current		V_{GD} = 5 V	µA			500
I_{gss}	Gate Leakage Current		$V_{GD} = V_{GS}$ = -4 V	µA	—	30	300
NF	Noise Figure	f = 2 GHz	V_{DS} = 4 V, I_{DS} = 60 mA	dB		0.5	0.8
			V_{DS} = 4 V, I_{DS} = 30 mA			0.5	
		f = 900 MHz	V_{DS} = 4 V, I_{DS} = 60 mA	dB		0.4	
G_a	Associated Gain	f = 2 GHz	V_{DS} = 4 V, I_{DS} = 60 mA	dB	16	17.5	19
			V_{DS} = 4 V, I_{DS} = 30 mA			17	
		f = 900 MHz	V_{DS} = 4 V, I_{DS} = 60 mA	dB		21.5	
OIP3	Output 3rd Order Intercept Point[3]	f = 2 GHz +5 dBm P_{out}/Tone	V_{DS} = 4 V, I_{DS} = 60 mA	dBm	29	31.5	
			V_{DS} = 4 V, I_{DS} = 30 mA			30	
		f = 900 MHz +5 dBm P_{out}/Tone	V_{DS} = 4 V, I_{DS} = 60 mA	dBm		31	
P_{1dB}	1 dB Compressed Intercept Point[3]	f = 2 GHz	V_{DS} = 4 V, I_{DS} = 60 mA	dBm		20	
			V_{DS} = 4 V, I_{DS} = 30 mA			19	
		f = 900 MHz	V_{DS} = 4 V, I_{DS} = 60 mA	dBm		18.5	

Notes:
1. Guaranteed at wafer probe level
2. Typical value determined from a sample size of 450 parts from 9 wafers.
3. Using production test board.

Figure C.1: *Specification sheet ATF34143, part 1*

ATF-34143 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain - Source Voltage[2]	V	5.5
V_{GS}	Gate - Source Voltage[2]	V	-5
V_{GD}	Gate Drain Voltage[2]	V	-5
I_D	Drain Current[2]	mA	I_{dss}[3]
P_{diss}	Total Power Dissipation[4]	mW	725
$P_{in\ max}$	RF Input Power	dBm	17
T_{CH}	Channel Temperature	°C	160
T_{STG}	Storage Temperature	°C	-65 to 160
θ_{jc}	Thermal Resistance[5]	°C/W	165

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. V_{GS} = 0 volts.
4. Source lead temperature is 25°C. Derate 6 mW/°C for T_L > 40°C.
5. Thermal resistance measured using 150°C Liquid Crystal Measurement method.
6. Under large signal conditions, V_{GS} may swing positive and the drain current may exceed I_{dss}. These conditions are acceptable as long as the maximum P_{diss} and $P_{in\ max}$ ratings are not exceeded.

Figure C.2: *Specification sheet ATF34143, part 2*

C.2 ATF35143

ATF-35143 Electrical Specifications

T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameters and Test Conditions			Units	Min.	Typ.[2]	Max.
I_{dss}[1]	Saturated Drain Current		V_{DS} = 1.5 V, V_{GS} = 0 V	mA	40	65	80
V_P[1]	Pinchoff Voltage		V_{DS} = 1.5 V, I_{DS} = 10% of I_{dss}	V	-0.65	-0.5	-0.35
I_d	Quiescent Bias Current		V_{GS} = 0.45 V, V_{DS} = 2 V	mA	—	15	—
g_m[1]	Transconductance		V_{DS} = 1.5 V, g_m = I_{dss}/V_P	mmho	90	120	—
I_{GDO}	Gate to Drain Leakage Current		V_{GD} = 5 V	µA			250
I_{gss}	Gate Leakage Current		V_{GD} = V_{GS} = -4 V	µA	—	10	150
NF	Noise Figure[3]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		0.4	0.7
			V_{DS} = 2 V, I_{DS} = 5 mA			0.5	0.9
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		0.3	
			V_{DS} = 2 V, I_{DS} = 5 mA			0.4	
G_a	Associated Gain[3]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB	16.5	18	19.5
			V_{DS} = 2 V, I_{DS} = 5 mA		14	16	18
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dB		20	
			V_{DS} = 2 V, I_{DS} = 5 mA			18	
OIP3	Output 3rd Order Intercept Point[4, 5]	f = 2 GHz	V_{DS} = 2 V, I_{DS} = 15 mA	dBm	19	21	
			V_{DS} = 2 V, I_{DS} = 5 mA			14	
		f = 900 MHz	V_{DS} = 2 V, I_{DS} = 15 mA	dBm		19	
			V_{DS} = 2 V, I_{DS} = 5 mA			14	
P_{1dB}	1 dB Compressed Intercept Point[4]	f = 2 GHz	V_{DS} = 2 V, I_{DSQ} = 15 mA	dBm		10	
			V_{DS} = 2 V, I_{DSQ} = 5 mA			8	
		f = 900 MHz	V_{DS} = 2 V, I_{DSQ} = 15 mA	dBm		9	
			V_{DS} = 2 V, I_{DSQ} = 5 mA			9	

Notes:
1. Guaranteed at wafer probe level
2. Typical value determined from a sample size of 450 parts from 9 wafers.
3. 2V 5 mA min/max data guaranteed via the 2V 15 mA production test.
4. Measurements obtained using production test board described in Figure 5.
5. P_{out} = -10 dBm per tone

Figure C.3: *Specification sheet ATF35143, part 1*

ATF-35143 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain - Source Voltage[2]	V	5.5
V_{GS}	Gate - Source Voltage[2]	V	-5
V_{GD}	Gate Drain Voltage[2]	V	-5
I_{DS}	Drain Current[2]	mA	I_{dss}[3]
P_{diss}	Total Power Dissipation[4]	mW	300
$P_{in\ max}$	RF Input Power	dBm	14
T_{CH}	Channel Temperature	°C	160
T_{STG}	Storage Temperature	°C	-65 to 160
θ_{jc}	Thermal Resistance[5]	°C/W	150

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Assumes DC quiesent conditions.
3. V_{GS} = 0 V
4. Source lead temperature is 25°C. Derate 3.2 mW/°C for T_L > 67°C.
5. Thermal resistance measured using QFI Measurement method.

Figure C.4: *Specification sheet atf35143 part 2*

C.3 Paris HEMTs

The specifications provided by Q. Dong and Y. Jin are given below. Important are the capacitances and the transconductances (they have a trade-off). Furthermore, the current and voltage noise are important.

It is also specified that the bias voltage should be 100mV and no more that 150mV.

H

Series number of supplied 5pF cryoHEMT is 13SE08 20150410. Characteristics at 4.2 K[A] and V_{ds}=100mV are:

Name	I_{ds} (mA)	V_{gs} (mV)	g_m (mS)	g_d (mS)	C_{gs} (pF)	C_{gd} (pF)	e_n@1kHz (nV/√Hz)	e_n@100kHz (nV/√Hz)	i_n@1kHz (aA/√Hz)	i_n@100kHz (fA/√Hz)	i_n@1MHz (fA/√Hz)
B1	1	-68.4[B]	44.5	1.51	4.6	1	1.6	0.28	70[C]	0.7[C]	2.2[C]
	0.5	-82.0[B]	30.0	0.77			2.1	0.31			
B2	1	-65.2[B]	43.0	1.54	4.6	1	1.3	0.26	70[C]	0.7[C]	2.2[C]
	0.5	-78.7[B]	28.8	0.77			1.3	0.29			

[A] DC characteristics remain almost unchanged at T≤ 4.2 K, noise characteristics can be improved.

[B] Please note that actual V_{gs} can vary few mV according to the cooling process.

[C] Results from a same HEMT with the same configuration.

Figure C.6: *Transistor B2 is used for the CS stage.*

Name		200pch	100pch	30pch	5pch	1pch
L_gxW (µm²)		1.5×10⁵	6.4×10⁴	2.0×10⁴	2.0×10³	4.0×10²
C_{gs} (pF); C_{gd} (pF)		236; 8.9	103; 8.9	33; 3.5	4.6; 1.0	1.8; ~0.6
V_{ds}(mV); I_{ds}(mA)		100; 1.0	100; 1.0	100; 1.0	100; 1.0	100; 0.5
g_m (mS); g_d (mS)		52; 0.4	40; 1.2	115; 1.3	44; 1.3	15; 0.8
$ft = g_m/(2\pi C_{gs})$ (Hz)		3.5×10⁷	6.2×10⁷	5.5×10⁸	1.5×10⁹	1.3×10⁹
e_n (nV/Hz½)	@1Hz @10Hz @100Hz @1kHz	5.4 1.7 0.52 0.24	6.3 2.1 0.76 0.34	14 4.5 1.5 0.57	30 12 4.5 1.4	100 30 10 2.7
$e_{n\text{-white}}$ (nV/Hz½)		0.18	0.22	0.12	0.21	0.4
i_n (aA/Hz½)	@1Hz @1kHz	21 6.8×10²	15 5.1×10²	9.1 2.4×10²	2.2 70	3.6 57
R_n (Ω)	@1Hz @1kHz	2.6×10⁸ 3.5×10⁵	4.2×10⁸ 6.3×10⁵	1.5×10⁹ 2.2×10⁶	1.4×10¹⁰ 2.0×10⁷	2.8×10¹⁰ 3.7×10⁷
T_{nt} (mK)	@1Hz @1kHz	4.1 5.9	3.4 6.2	4.6 5.0	2.4 3.6	13 5.6

Figure C.5: *Specification of various transisor types. The 5pnch is used for the CS an CG. The 30pnch is used for the CD.*

Parameters at 4.2 K and V_{ds}=100mV

30pch

	I_{ds}(mA)	V_{gs} (mV)	g_m (mS)	g_d (mS)	e_n(nV/Hz^{½}) @ 10Hz/1kHz	e_n(nV/Hz^{½}) @100kHz
A1	**1**	**-95.6**	**105.9**	**1.26**	**4.2/0.57**	**0.2**
	0.5	-101.4	69.8	0.77	4.9/0.66	0.22
A3	**1**	128.5	116.5	1.36	5.0/0.6	0.12
	0.5	134	75.8	0.81	5.5/0.65	0.126

5pch

	I_{ds}(mA)	V_{gs} (mV)	g_m (mS)	g_d (mS)	e_n(nV/Hz^{½}) @ 10Hz/1kHz	e_n(nV/Hz^{½}) @100kHz
C1	**1**	**-54,6**	**41,9**	**1,62**	**12/1,5**	**0,26**
	0.5	-67,8	28,6	0,89	12/1,4	0,29

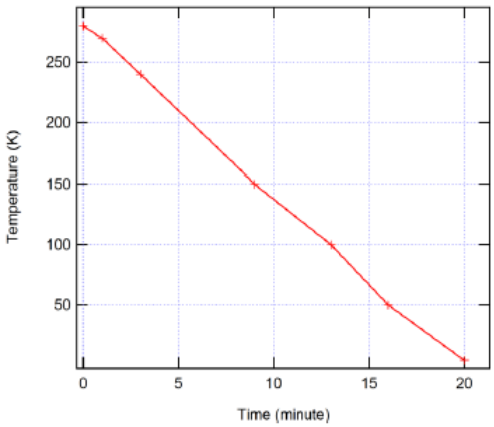
Figure C.7: *Transistor A1 is for the CD stage. Transistor C1 is for for the CG.*

H

- To avoid eventual degradation due to the heating, it is preferable to limit the soldering temperature below 250°C and the soldering time less than 5 minutes.

- To avoid eventual damage, please pay attention for cleaning the PCB circuit after soldering, i.e., do not put the cleaning solvent into the cavity of SOT23 (for more information, please ask us).

- To ensure the reproducibility of the bias voltage, the cooling rate is recommended to be not shorter than about 20 minute from 290 K to 4.2 K (see the figure below)



- During the cooling, we recommend to connect all circuits and just set the power supply voltage at 0V. If the gate is biased with a nonzero value or is left open during the cooling, you may encounter changes in V_{gs} for a chosen working point [see the reference APL 99, 113505 (2011)].

- In vacuum environment, experiences of preamplifiers by these cryoHEMTs show that no specific mounting is necessary for the thermal conductivity and metal wires connected to the transistor seem to be enough for the thermal dissipation of the power consumption of the transistor being equal to or below 100µW [see the supplementary material in Science 342, 601 (2013)].

- For the same series of cryoHEMTs, at deep cryogenic temperature and for a chosen working point i.e., a chosen V_{ds} and I_{ds}, the bias of V_{gs} can be different from one HEMT to another HEMT.

- During the operation under cryogenic conditions, if characteristics of the transistor have a significant variation, e.g., $|V_{gs}|$ being biased with 10 V, it is usually reversible, simply raising its temperature to room temperature and then cooling down to the working temperature. Usually, characteristics of a cryoHEMT remain unchanged with the gate bias $|V_{gs}| \leq 5$ V.

- To obtain the noise performance as in the datasheet, it is preferable to respect the indicated working point, i.e., I_{ds} and V_{ds}. When $V_{ds} > 150$ mV, it is possible to have higher noise values than these measured at $V_{ds} = 100$ mV.

Figure C.8: *Recommendations for using the transistors.*

C.4 Coil design

The design of the coil, as proposed by C. van Oosten is given in figure C.9.

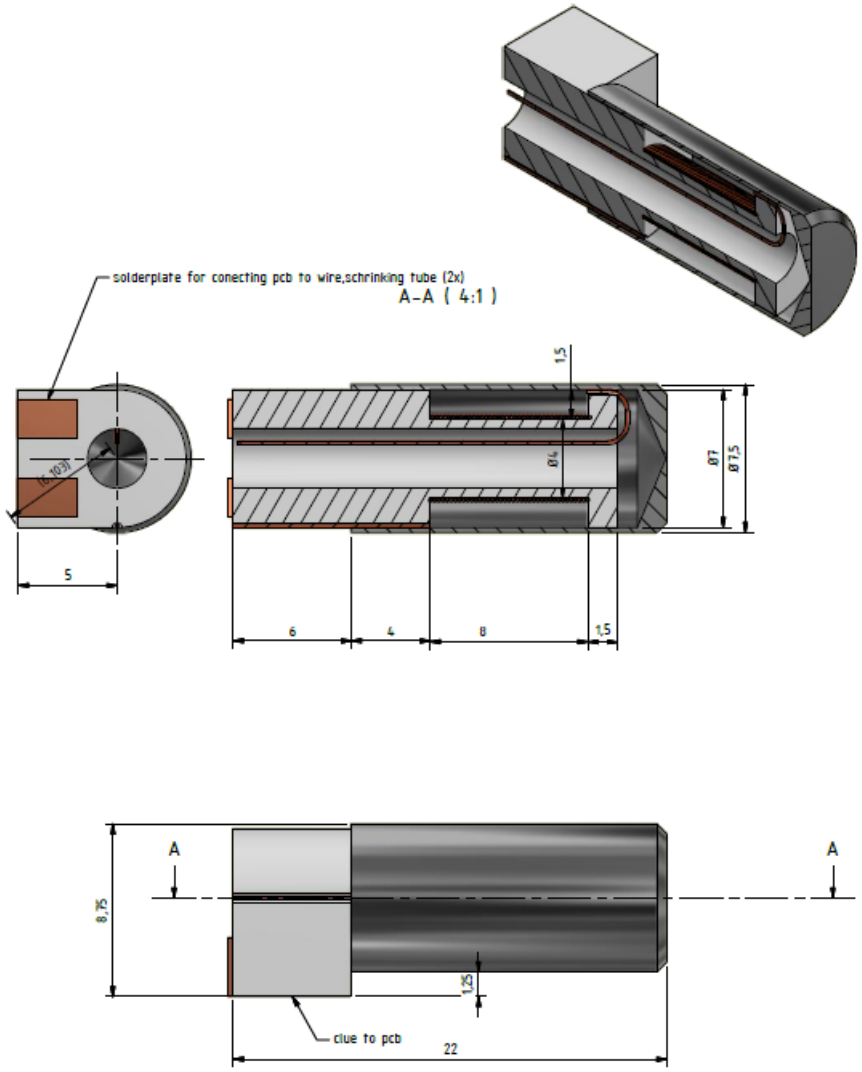


Figure C.9: *A schematic drawing of the design of the coil with shielding. The macor parts are in light grey. The niobium shielding is dark grey. The niobium wire is in brown.*

Appendix D

Transistor biasing

IV-curve for a typical commercial transistor is given here. Important is that the transistor biased properly and the current does not change much with the drain-source voltage. The measurements in the tests show this type of IV characteristic. ATF34143 shows a similar curve.

D.1 ATF35143

The IV curve of a commerical ATF35143 HEMT with a source resistance of 200Ω is given in figure D.1. This is a typical IV curve, measurement for all test set-ups from chapter 5.

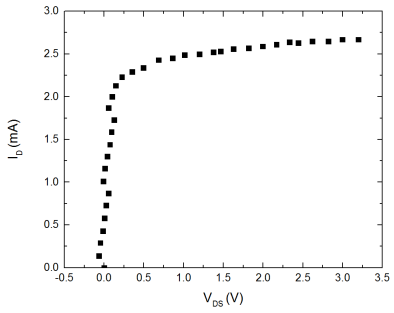


Figure D.1: *Typical IV curve of commercial transistor. This is the ATF35143 with a drain resistor of 200Ω*